TMS9995
Fastest 8/16-bit processor ever. With exclusive on-chip features.

from Texas Instruments.

With the TMS9995, Texas Instruments brings more speed and processing power to all those tough tasks that demand 16-bits. This ROM-less microcomputer supports low-cost, minimum chip count applications, historically supported by 8-bit CPUs, with the processing throughput of advanced 16-bit CPUs. And, like all 9900 Family CPUs, TMS9995 provides an advanced memory-to-memory architecture and compatible instruction set — all the way to the object code level — so you can move from one product level to another — from single chips to multi-chips to modules to systems — protecting your software and development systems investment as you go.

TMS9995. Superior functional performance at speeds 3 times faster than any previous 9900 Family processor.

TMS9995 — Key features

• 256 bytes of on-chip RAM • 12 MHz clock with on-chip clock generator • 8-bit data bus/16-bit address bus • 16-bit on-chip interval timer/event counter • Serial I/O via Communications Register Unit (CRU) • 7 prioritized vectored interrupts • 9900 Family instruction set including signed multiply and divide • Instruction prefetch • Automatic first wait-state generation • 64K bytes of memory address expansion • Single 5-volt operation • 40-pin package

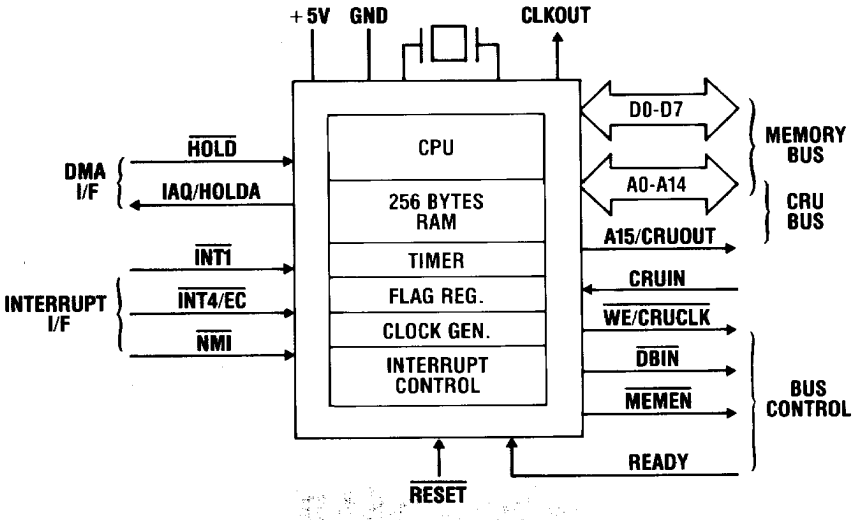


Figure 1 — TMS9995 Features and Signals

In addition to the 69 instructions of the TMS9900, four new ones have been added to enhance performance:

- A signed multiply (MPYS) that can process two signed 16-bit operands in 8.33 μs.
- A signed divide (DIVS) that can divide a 32-bit signed dividend by a 16-bit signed divisor in 11.0 μs.
- A load workspace pointer (LWP) which allows the workspace pointer to be loaded from a general memory location thus facilitating dynamic workspace allocation by ROM based firmware.
- A load status register (LST) which complements the load interrupt mask immediate (LIMI) by allowing the entire status word to be loaded from general memory. This facilitates reentrant ROM based firmware routines.

In addition to the TMS9995's rich native instruction set (see Table 1), a macro-instruction detect (MID) interrupt — a fetch and attempted execution of an opcode normally unused — opens the instruction set almost limitlessly. Unmaskable, the MID interrupt allows the emulation of user defined functions and allows the 9995 to execute the software of future 9900 Family processors.

For arithmetic intensive applications the 9995 provides an automatic arithmetic overflow interrupt eliminating time consuming "range checking" routines needed to guard against mid-routing overflow errors. The arithmetic overflow interrupt will occur when enabled and immediately following the arithmetic instruction which caused the overflow to occur. Unlike most CPU's which implement "Trap on Overflow" instructions, the 9995 will provide automatic interrupt processing saving memory space and execution time.

TABLE 3 — MULTIPLY AND DIVIDE

	UNSIGNED MULTIPLY (16 BIT X 16 BIT)	UNSIGNED DIVIDE (32 BIT ÷ 16 BIT)	SIGNED MULTIPLY (16 BIT X 16 BIT)	SIGNED DIVIDE (32 BIT ÷ 16 BIT)
TMS9995 EXECUTION TIME	7.67 μs	9.33 μs	8.33 μs	11.0 μs

TABLE 1 — TMS9995 INSTRUCTION SET

MNEMONIC	DESCRIPTION
A	Add Word
AB	Add Byte
ABS	Absolute Value
AI	Add Immediate
ANDI	And Immediate
B	Branch
BL	Branch and Link
BLWP	Branch and Load Workspace Pointer
C	Compare Word
CB	Compare Byte
CI	Compare Immediate
CKOF	External Clock Off
CKON	External Clock On
CLK	Clear Word
COC	Compare Ones Corresponding
CZC	Compare Zeros Corresponding
DEC	Decrement
DECT	Decrement By Two
DIV	Unsigned Divide
DIVS	Signed Divide
IDLE	Idle Processor
INC	Increment
INCT	Increment By Two
INV	Invert
JUMP	Jump (1-unconditional, 12-conditional)
LDCR	Load Communications Register Unit (I/O)
LI	Load Workspace Register Immediate
LIMI	Load Interrupt Mask Immediate
LREX	Load External
LST	Load Status Register
LWP	Load Workspace Pointer
LWPI	Load Workspace Pointer Immediate
MOV	Move Word
MOVE	Move Byte
MPY	Unsigned Multiply
MPYS	Signed Multiply
NEG	Negate
ORI	OR Immediate
RSET	External Reset
RTWP	Return to Workspace Pointer
S	Subtract Word
SB	Subtract Byte
SBO	Set Bit to One (I/O)
SBZ	Set Bit to Zero (I/O)
SETO	Set Word to Ones
SHIFT	Shift (4 versions)
SOC	Set Ones Corresponding (word)
SOCB	Set Ones Corresponding (byte)
STCR	Store Communication Register Unit (I/O)
STST	Store Status Register
STWP	Store Workspace Pointer
SWPB	Swap Bytes
SZC	Set Zeros Corresponding (word)
SZCB	Set Zeros Corresponding (byte)
TB	Text Bit (I/O)
X	Execute
XOP	Extended Operation (Software Context Switch-16 XOP's)
XOR	Exclusive-OR

TABLE 2 — ADDRESSING MODES

Workspace Register
Workspace Register Indirect
Workspace Register Indirect Auto Increment
Direct
Indexed
Immediate
PC Relative
CRU Relative (I/O instructions)

As the number of chips in a system directly impacts cost and reliability, the TMS9995 is designed to reduce the required number of packages in a system.

- Two hundred fifty-six (256) bytes of on-chip RAM eliminates the need for external RAM chips for many small-system applications.
- On-chip, crystal controlled clock generation eliminates the need for external clock generator chips.
- Separate address and data bus eliminates the need for external address latches required for multiplexing schemes.
- An interrupt controller/synchronizer is integrated on-chip to eliminate circuitry normally required to interface asynchronous interrupt pulses to the CPU (see Figure 2).
- The Communications Register Unit (CRU) address space has been expanded from the 9900's 4096 bits to 32,768 input and 32,768 output bits. Thus, for small systems a minimal amount of address decoding is needed externally.
- Timing functions such as event counting and interval timing are performed on-chip with a 16-bit decrementer. Configured as an event counter, the time resolution is 1.33 microseconds. As an event counter, the 9995 decrementer can accept asynchronous pulses with repetition rates as high as 1 MHz.
- A 16-bit flag register, in addition to providing timer control functions, provides flag bits to indicate presence of pending interrupts — allowing software to dynamically reprioritize the interrupts. Accessible via on-chip CRU address space, eleven user-definable flag bits may be used for inter-program semephore interaction or parameter passing capability.

With many of the system functions on-chip, the 9995 can support a flexible system with as little as three chips (see Figure 3). With 64K bytes of memory address expansion and 32K bits of CRU address expansion, the 9995 provides the hooks necessary to support larger, more complex systems as your applications grow. No matter how large or small the system, the processor must perform — and the TMS9995 does. In addition to the many features integrated on chip the 9995's architecture has been streamlined and optimized for high throughput performance.

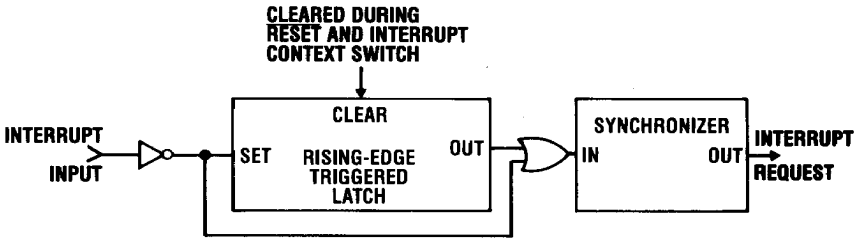


Figure 2 — Interrupt Inputs

The on-chip RAM, in addition to eliminating the need for a RAM chip in many minimal-chip applications, enhances performance by accessing a full 16-bit word in a single clock cycle. Since the external data bus on the 9995 is 8-bits, this internal access capability represents a definite performance enhancement to access frequently used workspace register contents.

For access to external memory devices, an automatic first wait state feature has been included in the 9995 to automatically inject the first wait state in each external memory operation. One wait state memory cycles permit the 9995 to use 450 nanosecond access (read) and 667 nanosecond cycle time memories — most of the low cost memories available today. For maximum performance requirements, the 9995 can access memory with no wait states for a fast access time of 120 nanoseconds and cycle time of 330 nanoseconds. Thus a TMS9995 system can utilize the best memories, in terms of speed and cost, for a given application.

To further enhance the high performance and memory bandwith capability of the 9995, an intelligent prefetch scheme has been incorporated into the architecture to better utilize the memory bus — usually the limiting factor to performance in CPU operation. During internal ALU cycles in which the memory bus in usually inactive, the 9995 is fetching the next instruction. Prefetch is made intelligent by fetching the proper address in the case of jump or branch instructions.

All these enhancements add up to performance. Table 4 lists the performance of 9995 as benchmarked against the Intel 8088 and the Motorola 6809. The particular benchmark algorithms are those used by Intel Corporation[1].

[1]Intel application note AFN01551A, Intel Corporation, Santa Clara, California 1980.

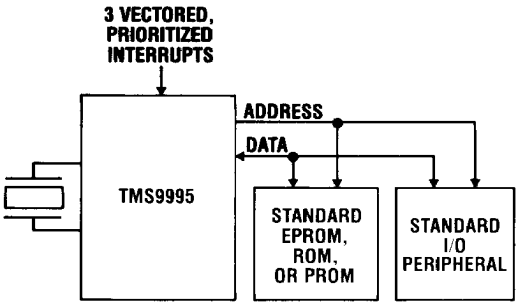


Figure 3 — TMS9995 Minimum System Configuration

TABLE 4 — BENCHMARKS

	AUTOMATED PARTS INSPECTION (sec)	COMPUTER GRAPHICS XY TRANSFORM (sec)	BUBBLE SORT (ms)	BLOCK TRANSLATION (ms)	16 BIT MULTIPLY (μs)	SINGLE VECTORED INTERRUPT (μs)
9995 (12 MHz) w/120ns PROM	0.666	0.863	1.240	1.767	10.00*	8.00
9995 (12 MHz) w/450ns EPROM	0.950	1.081	1.956	2.696	12.67	10.67
8088 (5 MHz) w/450ns EPROM	1.596	2.402	2.254	1.522	40.8	77.6
6809 (2 MHz) w/450ns EPROM	9.67	57.1	2.376	3.01	91.9	27.6

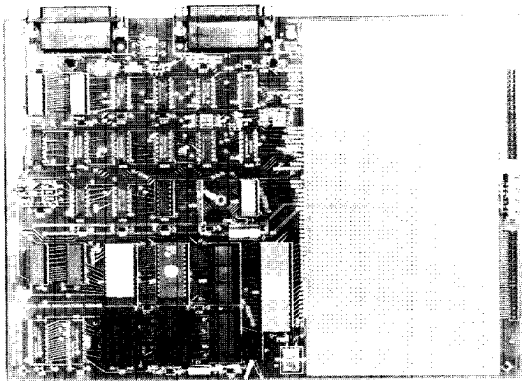
*7.67 μs if multiplicands don't have to be saved.

TABLE 5 — 9900 FAMILY PERIPHERALS

TMS9901	Programmable Systems Interface
TMS9902A	Asynchronous Communications Controller
TMS9903	Synchronous Communications Controller
TIM9905	Data Selector/Multiplexer
TIM9906	8-bit Addressable Latch
TIM9907/8	Priority (Interrupt) Encoders
TMS9909	Floppy Disk Controller
TMS9914A	GPIB Adaptor
TMS9918A	Color Video Display Processor
TMS9927	Video Timer/Controller
TIM99600	Memory Refresh Controller
TIM99610	Memory Mapper
TIM99630	Error Detection and Correction Circuit

Advanced Peripheral Support

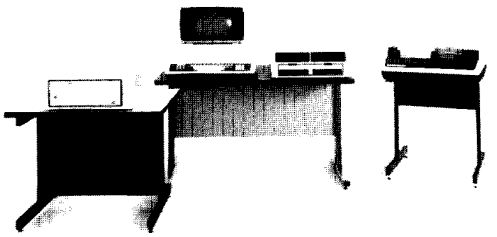
The TMS9995, as well as all 9900 family CPU's, is supported by an established and proven family of advanced VLSI peripheral devices. The TI 9900 family of LSI peripherals contains a wide selection of system support circuits used to easily and cost effectively perform peripheral and interface functions such as data communications, memory functions, special signal processing, and display. Included are controllers, latches, multiplexers, encoders and others. The bus structure, architecture, I/O features, and other characteristics of these peripheral and interface circuits are totally compatible with other members of the 9900 family. Fully supported by software, software development systems, and TI's technical assistance, these circuits are available now. And, as additional peripheral and interface circuits are added to the 9900 family, they too will be fully compatible with existing members. A list of these powerful family peripherals is given in Table 5.



TMS9995 Evaluation Support

The TMS9995 evaluation model (TMAM6095) is a stand alone microcomputer board that supports evaluation of TMS9995 software and hardware features as well as prototyping of TMS9995 interfaces. This module contains a powerful monitor that enables programs to be assembled, edited, and executed. The powerful symbolic assembler also provides reverse assembly capability. Hardware features include two EIA data communication links that provide for interface to a local terminal and to a host system for upload/down-load capability. In addition to the 256 bytes of on-chip RAM provided by the TMS9995, 1K bytes of external RAM is populated. Six kilobytes of EPROM is populated containing the monitor and assembler; however, up to 24K of EPROM may be used by populating the three 28-pin sockets with TMS2564 EPROMs. Personality modules for each of the three 28-pin sockets may be configured to allow use of virtually any X8 organized memory. A large prototyping area provides ample room for breadboarding of TMS9995 systems.

AMPL System — Advanced Microprocessor Prototyping Lab



The AMPL system is a complete set of software and hardware tools that maximize software productivity for the entire 9900 family.

AMPL includes a video display terminal, hard disk or floppy diskette mass storage and extensive software. The lab is available as a floppy disk system or as a multi-user hard-disk system. Programs can be edited, assembled, loaded and executed with easy, self-prompting commands.

The logic-state trace features inactive on-line control and analysis to provide fast data reduction and programmable emulation control based on the result of this analysis. AMPL uses a high-level language with designed-in features to simplify orientation for the new user, while providing extensive flexibility and support for the experienced user. PROM programming implements target system memory in PROM and EPROM while AMPL interactive process makes it easy to identify and implement needed sign design changes.

Microprocessor Pascal System

TI's Microprocessor Pascal system, developed for the 16-bit 9900 Family, provides an increased applications capability and decreases development time. TI Microprocessor Pascal is third-generation Pascal resulting from TI's pioneering efforts with the language. It allows designers to solve applications problems without becoming involved with the intricacies of machine architecture. The code is easier to write, document, read, and modify, and results in fewer programming errors. Direct CRU commands are available for direct bit and byte manipulation. Microprocessor Pascal has concurrency extensions particularly suitable for realtime multitasking applications.

TI's Microprocessor Pascal system consists of six parts:

- **Source Editor** — Specifically designed to create/edit Pascal programs and check program syntax before compilation.
- **Compiler** — Compiles conventional Pascal programs as well as TI's Pascal concurrent extensions into interpretive code, which can then be executed directly or converted to 9900 native machine code.
- **Host Debugger** — More than 15 options for tracing variables and modifying data.
- **Configurator** — Enables the target system to retain only the part of the runtime support necessary for program execution.
- **Run-Time Support** — Both interpretive and native-code execution provide a speed/memory tradeoff.