The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

TM 990/305 COMBINATION MEMORY AND I/O EXPANSION MODULE

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SECTION 1

INTRODUCTION

1.1 GENERAL

The TM 990/305 is a combination memory and input/output expansion module. This module can comprehend a 16-bit address, as used in a TM 990/10X system, or a 20-bit address, as used in a system utilizing a memory-mapping CPU. The TM 990/305 has a memory capacity of 32K bytes. Memory configuration is significantly enhanced by allowing the use of either static RAM or EPROM in each of the memory sockets. This module has 16 parallel input channels (Port 1) and 16 parallel input/output channels (Port 0) that can be configured individually as either inputs or outputs. All I/O channels are optically isolated and interface through the Communications Register Unit (CRU).

Input/output flexibility is designed into the TM 990/305 to allow the user to configure the I/O channels to meet his requirements. Input channels may be configured for input voltages up to 30 V, while output channels may be configured for TTL compatibility or as current drivers. Output channel polarity can be selected by the user as either inverting or non-inverting. For details, refer to Sections 4 and 6.

5MT industrial I/O interface capability is provided on the TM 990/305 module. An on-board voltage regulator supplies the required +8 V V_{CC} while the required pullup resistors for the I/O channels can be installed in sockets provided on the module. A TM 990/509 cable is then required to connect the TM 990/305 to a 5MT I/O system. Selection and placement of the proper resistors are explained in Section 6.10.5 and the appropriate interconnections are shown in Appendix F.

The TM 990/305 module offers the following features:

- Compatible with the TM 990 microcomputer system bus
- Designed to fit either the TM 990/510 or TM 990/520 card cage
- Designed to interface with the TM 990/100 or /101 CPU modules
- 16 or 20-bit address handling capability
- Memory capacity of 16K bytes (using TMS 4016 RAMs or TMS 2516 EPROMs)
- Memory capacity of 32K bytes (using TMS 2532 EPROMs)
- Jumper/wirewrap decoder to permit easy reassignment of memory map configuration
- 16 optically-isolated parallel input channels
- 16 optically-isolated parallel input/output channels, user-configurable
- Capability of reconfiguring input channels for voltages up to 30 V

- Output channels may be configured for TTL compatibility or as current drivers
- Switch selection to permit easy reselection of CRU base address
- 4 edge-triggered, latched interrupts user-configurable to interrupt levels 1-15
- 5MT interface capability using TM 990/509 cable assembly.

1.2 MANUAL ORGANIZATION

This manual is organized as follows:

- Section 1 covers module specifications and characteristics.
- Section 2 explains how to install and check out the TM 990/305 module.
- Section 3 covers memory placement and selection.
- Section 4 covers input/output port configurations.
- Section 5 presents the fundamental concepts involved in I/O and interrupt programming.
- Section 6 covers theory of operation, explaining the hardware design, configuration and circuitry.

1.3 MODULE CHARACTERISTICS

Figure 1-1 shows the principal components and interfaces of the TM 990/305 module. The system bus connector is P1, which is a 100-pin (50 each side) PC board edge connector spaced on 0.125 inch centers. Connector P2 interfaces with Port 0 and P3 interfaces with Port 1. A ribbon or twisted-pair cable with a 40-pin, 0.1-inch center spacing PCB edge connector will be required for each port used.

Figure 1-2 shows the PC module silkscreen markings which detail the various components on the module; also included are the module dimensions and tolerances.

1.4 GENERAL SPECIFICATIONS

- Power Requirements: +5 V $\pm$ 3%, 1.5 A.

  To interface with a 5MT industrial control system, a +12 V $\pm$3%, 0.75 A power supply is required.

- Operating Temperature: 0°C to 70°C.
- Module Dimensions: See Figure 1-2.

- Memory Capacity:*

  a. RAM: 16K bytes using TMS 4016 static RAMs
  b. EPROM: 16K bytes using TMS 2516 EPROMs
  32K bytes using TMS 2532 EPROMs.

- Input/Output Capability:**

  a. Port 0: 16 parallel input/output channels (optically-isolated)
  b. Port 1: 16 parallel input channels (optically-isolated).

NOTES

* The TM 990/305 module is shipped with memory sockets only; no memory devices are shipped.

** The TM 990/305 module is shipped with 16 input opto-couplers and 4 output opto-couplers in Port 0. No opto-couplers are shipped in Port 1.

1.5 APPLICABLE DOCUMENTS

- TMS 9900 Microprocessor Data Manual
- TM 990/100 or /101 Microcomputer User's Manual
- Model 990 Computer TMS 9900 Microprocessor Assembly Language Programmer's Guide
- The MOS Memory Data Book, 1979 Edition
- The Optoelectronics Data Book
- 9900 Family Systems Design and Data Book

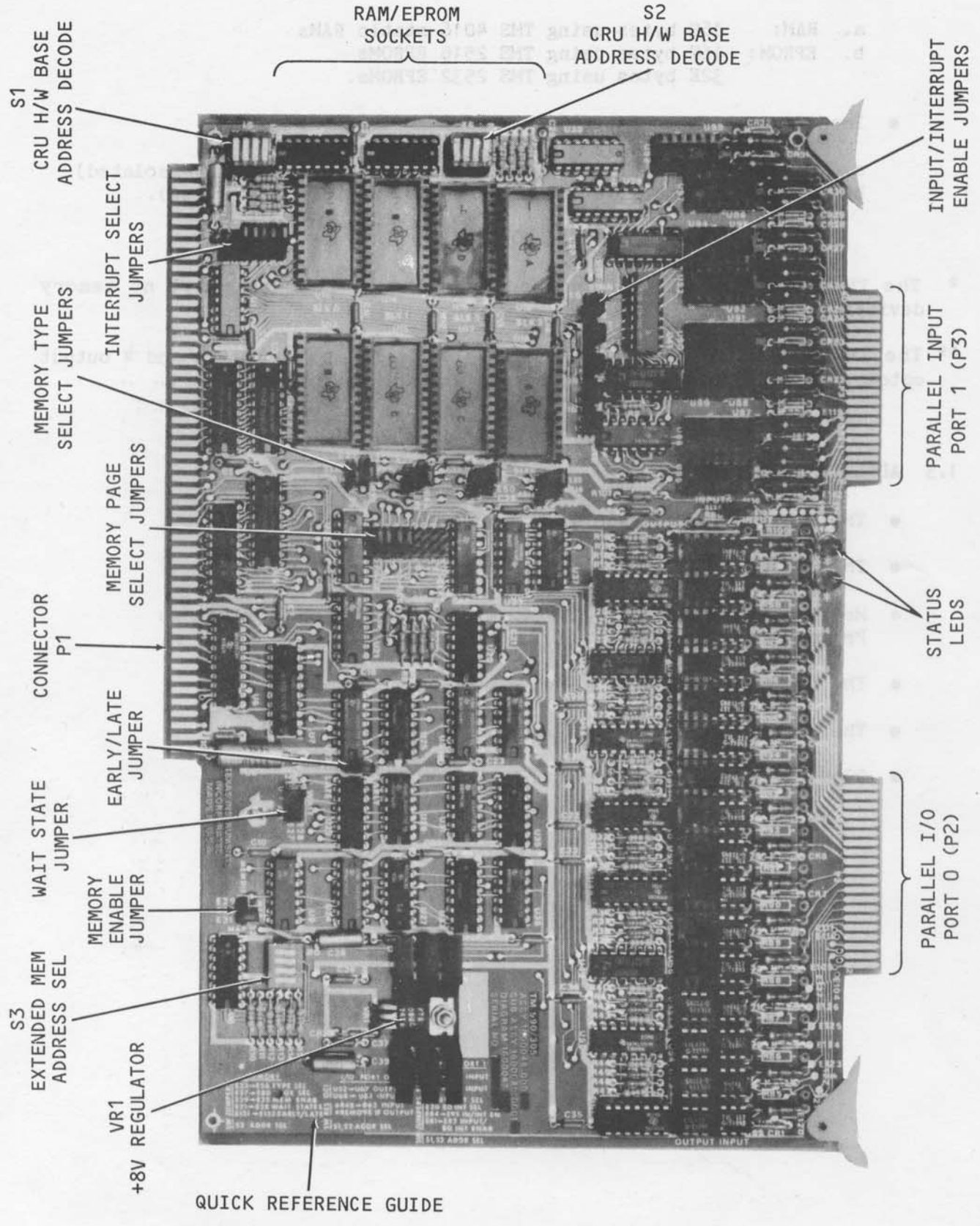
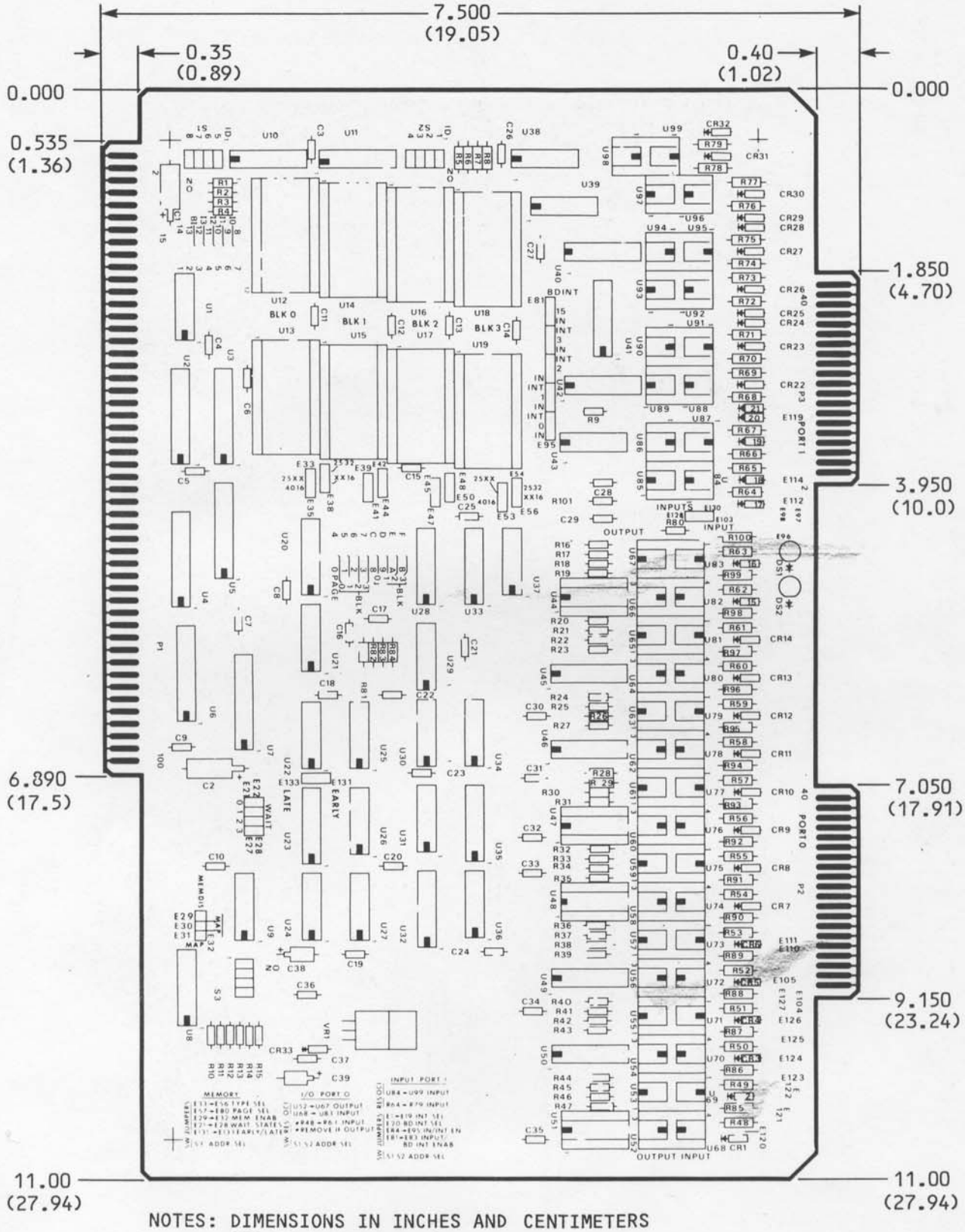


FIGURE 1-1. TM 990/305 PRINCIPAL COMPONENTS



NOTES: DIMENSIONS IN INCHES AND CENTIMETERS
(CM IN PARENTHESES)

FIGURE 1-2. TM 990/305 MODULE DIMENSIONS

SECTION 2

INSTALLATION AND CHECKOUT OF TM 990/305 MODULE

2.1 GENERAL

The following topics are described in this section:

- Equipment required for TM 990/305 module operation
- Unpacking and inspection
- Jumper configuration
- Switch configuration
- Power supply connections
- Operational checkout.

It is presumed that the user is familiar with the hardware and programming of the host microcomputer. This data is available in the TM 990/100 or /101 Microcomputer User's Guide.

2.2 REQUIRED EQUIPMENT

The basic equipment required to use a TM 990/305 module in a microcomputer system is described in the following paragraphs.

2.2.1 Host Microcomputer

The TM 990/305 module can be used with either the TM 990/100 or TM 990/101 CPU modules or a memory-mapping CPU module.

2.2.2 Terminal Device

Any RS-232-C device operable at a baud rate acceptable to the software being used or an ASR33 Teletype modified for 20 mA current loop operation interfaced to the CPU module can be used. TIBUG software supplies 110, 300, 1200 and 2400 baud, and certain versions provide additional rates such as 9600 or 19200 baud.

2.2.3 Power Supply

A dc power supply capable of supplying +5 Vdc @ 1.5 A is required. When interfacing with a 5MT system, a +12 Vdc @ 0.75 A power supply is required.

2.2.4 Card Cage/System Bus Connector

Use of either the TM 990/510 or TM 990/520 card cage greatly facilitates operation and setup. The TM 990/305 communicates with the CPU module via the 100-pin bus interface socket of the card cage. Alternately, one of the following 100-pin, 0.125 inch (center-to-center) PCB edge connectors may be used to interface with connector P1. Appropriate wire-wrap connector types

are listed below:

- TI H321150
- Amphenol 225-804-50
- Viking 3VH50/9CND5

2.2.5 Parallel I/O Connector

I/O interface is accomplished through connectors P2 and P3. P2 interfaces with Port 0 and P3 interfaces with Port 1. A ribbon or twisted-pair cable with a 40-pin, 0.100 inch center spacing PCB edge connector will be required for each port used. Appropriate connector types are given below:

- TI H312120 (Solder Tail)
- Viking 3VH20/1JN5 (Pierced Tail)
- 3M 3464-0001 (Ribbon Cable)

2.3 UNPACKING AND INSPECTION

Remove the TM 990/305 module from its carton and remove the protective wrapping. Check the module for shipping damage. If any damage is found, notify your TI distributor.

2.4 JUMPER CONFIGURATION AS SHIPPED

Check the module and verify that the jumper configuration is as described in Table 2-1.

TABLE 2-1. MODULE JUMPER POSITIONS AS SHIPPED

FUNCTION	STAKE PINS USED	PROPER CONNECTION & DESCRIPTION
CPU Interrupt Levels 1-15	E1 through E15	E8 to E16 (Level 8 to Source 0)
Interrupt Sources 0-3	E16 through E19	E9 to E17 (Level 9 to Source 1)
		E10 to E18 (Level 10 to Srce 2)
		E11 to E19 (Level 11 to Srce 3)
Board interrupt Source	E20, E134	E12 to E20 (Level 12 to Bd Int)
Memory Wait States	E21 through E28	E21 to E22 No Wait States
Memory Enable	E29 through E32	E30 to E32 Enable memory for /100 or /101 CPU
Memory Type Select BLK0	E33 through E38	E34 to E35, E37 to E38 TMS 4016
BLK1	E39 through E44	E40 to E41, E43 to E44 TMS 4016
BLK2	E45 through E50	E46 to E47, E49 to E50 TMS 4016
BLK3	E51 through E56	E52 to E53, E55 to E56 TMS 4016
Memory Page Select	E57 through E80	E61 to E73, (Page 4 to Block 0)
		E62 to E74, (Page 5 to Block 1)
		E63 to E75, (Page 6 to Block 2)
		E64 to E76, (Page 7 to Block 3)
Input/Board Int Enable	E81 through E83	E82 to E83 Input Enabled
Input/Interrupt 0 Enable	E84 through E86	E85 to E86 Input Enabled
Input/Interrupt 1 Enable	E87 through E89	E88 to E89 Input Enabled
Input/Interrupt 2 Enable	E90 through E92	E91 to E92 Input Enabled
Input/Interrupt 3 Enable	E93 through E95	E94 to E95 Input Enabled
Memory Early/Late	E131 through E133	E131 to E132 Early
5MT +5 V	E128 through E130	E128 to E129 Not Selected

2.5 SWITCH CONFIGURATION AS SHIPPED

The TM 990/305 is shipped with the switch configuration shown in Table 2-2.

TABLE 2-2. SWITCH CONFIGURATION AS SHIPPED

FUNCTION	SWITCH DESIGNATION	PROPER SETTING AND DESCRIPTION	
		ID5 ID6 ID7 ID8	
CRU Hardware Base Address (2nd least significant digit)	S1 (4-position)	ON ON ON ON	H/W Base Address = 0100_{16}
		ID1 ID2 ID3 ID4	
CRU Hardware Base Address (3rd least significant digit)	S2 (4-position)	ON ON ON OFF	H/W Base Address = 0100_{16}
		ID1 ID2 ID3 ID4	
Extended Mem. Addr. Decode	S3 (4-position)	X X X X	X = Don't care

2.6 POWER SUPPLY CONNECTIONS

If a TM 990/510 or TM 990/520 card cage is used, power supply connections can be made at terminal block (TB1) on the back of the card cage. Connect +5 Vdc to TB1-6 and the power supply ground to TB1-1 or TB1-10. If +12 V is required (for 5MT interface), connect +12 Vdc to TB1-5.

CAUTION

Always turn off the power supply before installing or removing the TM 990/305 module. Failure to observe this precaution may result in damage to the module.

2.7 INSTALLATION

The following procedure is for a TM 990/305 module used with a TM 990/100 or /101 CPU (With TIBUG installed in EPROM):

a. Install the TM 990/100 or /101 and TM 990/305 modules in the card cage. Attach the terminal connector to J2 on the TM 990/100 or /101 CPU module.

b. Power up the terminal device and switch on the power supplies.

c. Actuate the RESET switch on the TM 990/100 or /101 CPU module and press the letter A key or a carriage return (CR) on the terminal device. TIBUG, the debug monitor program, will output an initialization message.

2.8 OPERATION

Two test procedures will be given that allow the user to check out the initial performance of the TM 990/305 with a TM 990/100 or /101 CPU module installed (with TIBUG in EPROMs). The first test routine will verify satisfactory I/O

operation and the second routine will evaluate memory expansion operation. Both test routines are accomplished by using the TIBUG CRU Inspect (C command) and Memory Inspect (M command).

2.8.1 I/O Verification

This routine will lead to the verification of channel 0 of Port 0. A generalization of the test procedure that can be applied to the remainder of the channels is given at the end of this routine.

a. Ensure that the CRU hardware base address, which is governed by switches S1 and S2 on the TM 990/305 module, is set at >0100. This will configure bit 0 of Port 0 to have a software base address of >0200 (See Figure 5-4).

b. Install a user-suplied 140 ohm, 0.5 watt pullup resistor in socket position R85.

c. Connect a temporary jumper from pin 4 of U52 to pin 100 (ground).

d. Position a jumper plug on stake pins E129-E130 to connect +5 V to R85.

e. Repeat a, b, and c of Section 2.7.

f. Execute the following steps via the terminal device to verify the operation of channel 0 of Port 0. Underlines indicate user input at keyboard to check and change values at CRU bits. <CR> indicates a carriage return input.

Input/Output At Keyboard		Comments
? C 200,1<CR>		Inspect bit 0 of Port 0
0200 = 0000	1 <CR>	Set bit 0 to a "1'
? C 200,1<CR>		Inspect bit 0 of Port 0
0200 = 0001	0 <CR>	Bit 0 read matches the above output, set bit 0 back to "0"
? C 200,1<CR>		Inspect bit 0 of Port 0
0200 = 0000<CR>		Bit 0 read matches the above output

NOTE

Due to the comparatively slow switching time of opto-isolators, the space bar cannot be used after entering data to verify the contents. If used, the operator must enter two spaces and the second set of contents printed by TIBUG will be correct.

These steps verify that channel 0 of Port 0 is functionally operational. All other channels of Port 0 can be verified similarly by:

1. Ensuring the channel to be verified is populated with both an input TIL117 opto-isolator and an output TIL119 opto-isolator (See Section 6.10).

2. Installing a 140 ohm, 0.5 watt pullup resistor in the appropriate sockets (R86-R100) of the channel to be verified.

3. Connecting a temporary jumper from pin 4 of the appropriate output opto-isolator (U53-U67) to pin 100 (ground).

4. Repeat the above routine with the following adjustment in the C command to address the channel intended to be tested.

? C $ADDR_{16}$,1 CR

Where $ADDR_{16}$ = $(SFTWR\ BASE\ ADDRESS)_{16} + 2n$

$0 \leq n \leq F_{16}$

Channel number

2.8.2 Memory Verification

The memory sockets on board the TM 990/305 module will accept either static RAM or EPROM devices, which include TMS 4016, TMS 2516, and TMS 2532. Depending on the availability of the type of devices, the user can verify the memory operation by exccuting the following routine. Each individual block of memory, BLK0-BLK3, must contain the same device types installed in the pair of sockets provided; but different blocks may contain different mixtures of the allowable devices.

a. Populate (onboard the TM 990/305 module) at least one block of memory with the homogeneous type of devices mentioned above.

b. Position a jumper plug on stake pins E30 and E32 on the TM 990/305 module to enable memory expansion onboard (See Figure 3-5).

c. Position correctly two jumper plugs per block of memory selected for RAM or EPROM. As an example, assume that it is desired to populate memory BLK 0, BLK 1 and BLK 2 with three different types of memory devices in the following order.

   1. Static RAMs TMS 4016 in BLK 0, consisting of U12-U13.

   2. EPROMs TMS 2516 in BLK 1, consisting of U14-U15.

   3. EPROMs TMS 2532 in BLK 2, consisting of U16-U17.

   The correct jumper positions will be:

   1. E34-E35 and E37-E38 for BLK 0

   2. E39-E40 and E43-E44 for BLK 1

3. E45-E46 and E48-E49 for BLK 2

For further details see Table 3-1.

d. Configure the selected block(s) of memory into the memory map as desired by connecting the page select lines with either jumper plugs or wire-wrapped where required. For example, it is further desired to map all the memory devices mentioned in 2.8.2c into addresses above M.A.>2000. One possible configuration is to map BLK 0, BLK 1, and BLK 2 contiguously into addresses starting at M.A.>2000. This configuration would require the following connections to be made correctly in the page select jumper/wire-wrap area:

1. BLK 0 to Page 2

2. BLK 1 to Page 3

3. BLK 2 to Page 4 and Page 5

For further details refer to Section 3.4 and Section 6.6.1.

e. Repeat a, b, c of Section 2.7.

f. Depending on the type of devices populated, execute either or both of the routines listed below. Underlines indicate user input at keyboard to check and change contents of memory. CR indicates a carriage return. <SP>means space bar. <-> means a minus sign or hyphen. L_{16} is the address in memory (in hexadecimal) to be inspected.

2.8.2.1 For RAM Devices Populated Onboard

Input/Output At Keyboard		Comments
? M L_{16}<CR>		Inspect memory content at location L_{16}
L_{16} = XXXX	AAAA<SP>	Set contents at L_{16} = >AAAA
L_{16}+ 2 = YYYY	<->	Minus sign displays L_{16}
L_{16} = AAAA	5555<SP>	Content matches with what is set above change content to >5555
L_{16}+ 2 = YYYY	<->	Minus sign displays L_{16}
L_{16} = 5555<CR>		Content matches with what is set

These steps verify that the read and write operations at location L_{16} are basically functioning. The user can repeat the above steps at various locations as desired.

2.8.2.2 For EPROM Devices Populated Onboard

Input/Output At Keyboard	Comments
? M L_{16}<CR>	Inspect memory contents at location L_{16}
L_{16} = XXXX <SP>	The content at L_{16} = >XXXX is output
L_{16}+ 2 = YYYY <SP>	The content at L_{16}+ 2 =>YYYY is output
.	
.	
.	

These steps will allow the user to read the contents of the EPROMs at various locations for verification of correct data. Note that the M command cannot be used to write to EPROM, by definition.

SECTION 3

MEMORY PLACEMENT AND SELECTION

3.1 GENERAL

The TM 990/305 module provides memory expansion using either TMS 2516 EPROM, TMS 2532 EPROM, or TMS 4016 static RAM memory devices. The memory expansion section can comprehend either a 16 or a 20-bit address and provides multiple memory-wait states to accomodate the use of slower memories.

This section includes the following topics:

- Memory placement
- Memory selection
- Memory map configuration.

3.2 MEMORY PLACEMENT

Memory devices may be placed in sockets U12-U19. The smallest allowable partition will be a block of two homogenous devices configured in byte-parallel format. Figure 3-1 shows the block arrangement of memory sockets. The even-numbered sockets represent the most significant byte, i.e., U12, U14, U16, and U18 represent data bits D0-D7 of their respective block.

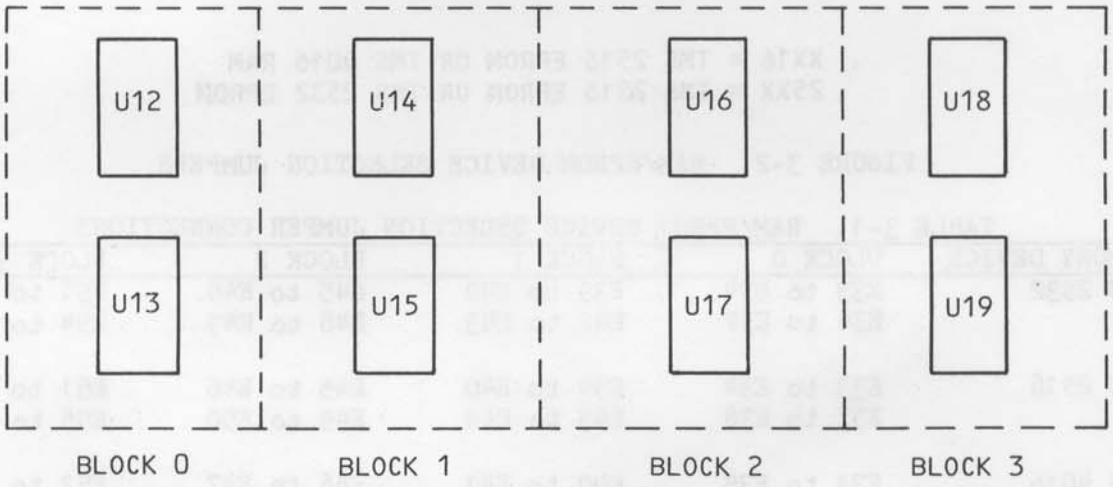


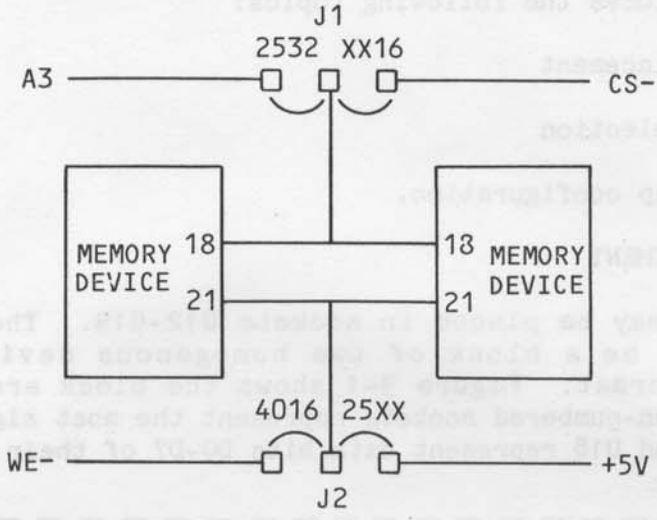
FIGURE 3-1. BLOCK ARRANGEMENT

The memory expansion sockets can be populated with all RAM devices, all EPROM devices, or a combination of both RAM and EPROM devices. The only constraint is that both devices comprising a block be of the same kind, since the two in parallel constitute a 16-bit word. As an example, block 0 (U12,U13) could be populated with TMS 4016 RAMs, block 1 (U14,U15) could be populated with TMS 2516 EPROMs, and blocks 2 (U16,U17) and 3 (U18,U19) could be populated with TMS 2532 EPROMs. It should be apparent that any number of memory device combinations are thus possible - this feature allows maximum system flexibility.

3.3 MEMORY SELECTION

3.3.1 Memory Type

In order to select EPROM or RAM memory, two jumper plugs per memory block must be positioned correctly (See Figure 3-2). The first jumper (shown here as J1) selects the proper signal for either a TMS 2532 EPROM or a TMS XX16 memory device. The second jumper (shown as J2) selects the proper signal for either a TMS 4016 RAM or a TMS 25XX memory device. The necessary jumper connections that are required to select EPROM or RAM memory devices are listed in Table 3-1.



XX16 = TMS 2516 EPROM OR TMS 4016 RAM
25XX = TMS 2516 EPROM OR TMS 2532 EPROM

FIGURE 3-2. RAM/EPROM DEVICE SELECTION JUMPERS

TABLE 3-1. RAM/EPROM DEVICE SELECTION JUMPER CONNECTIONS

MEMORY DEVICE	BLOCK 0	BLOCK 1	BLOCK 2	BLOCK 3
TMS 2532	E33 to E34 E36 to E37	E39 to E40 E42 to E43	E45 to E46 E48 to E49	E51 to E52 E54 to E55
TMS 2516	E33 to E34 E37 to E38	E39 to E40 E43 to E44	E45 to E46 E49 to E50	E51 to E52 E55 to E56
TMS 4016	E34 to E35 E37 to E38	E40 to E41 E43 to E44	E46 to E47 E49 to E50	E52 to E53 E55 to E56

3.3.2 Memory Page Select

As shown in Figure 3-3, memory address decoding yields 16 page select lines (Page 0 through Page F). A page is defined as a segment of 4K contiguous bytes within a selectable address range. Those page select lines are brought out to a jumper/wire-wrap area (Reference Figure 3-4) where they are configured by the user according to the desired memory map configuration (A discussion of memory map configuration is contained in Section 3.4 of this manual). Blocks 0-3 are connected to the page select lines by either jumper plugs or wire-wrapped where required. Notice that since the TMS 2532 EPROM pair consists of 8k bytes, it occupies <u>two</u> pages of addressing. Connections should be made appropriately.

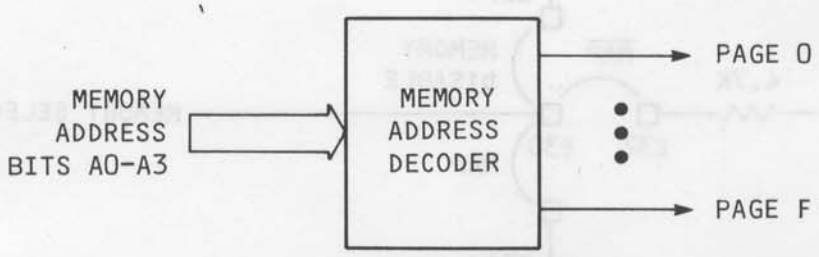
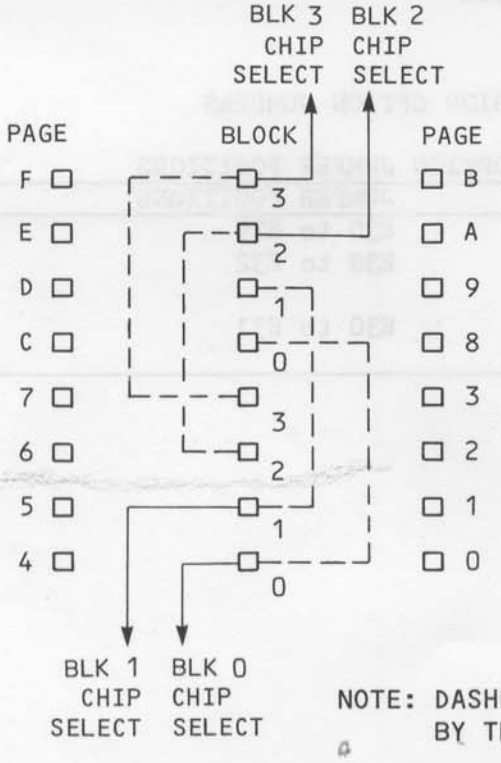


FIGURE 3-3. PAGE GENERATION



NOTE: DASHED LINES REPRESENT STAKE PINS CONNECTED BY THE BOARD'S PRINTED CIRCUITRY

FIGURE 3-4. JUMPER/WIRE-WRAP AREA

3.3.3 Memory Enable

Provision is made so that the memory expansion section on the TM 990/305 can be: 1. disabled, 2. used with the TM 990/100 or TM 990/101 CPU modules, or 3. used with a 20-bit address memory-mapping CPU module.

Figure 3-5 shows the jumper connections that determine which of the three aforementioned options is implemented and Table 3-2 shows the jumper positions needed to execute each option.

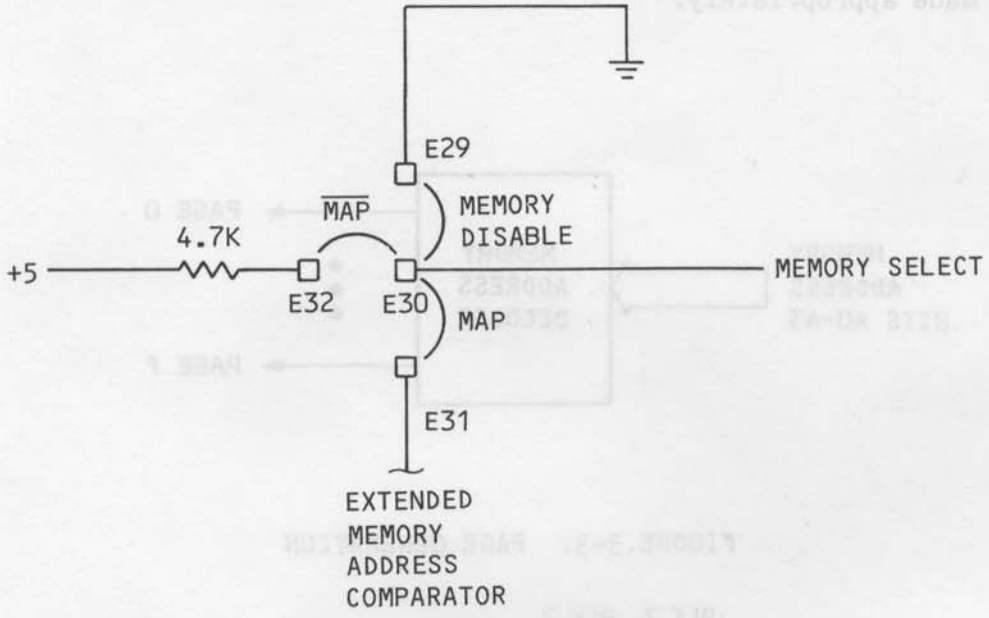


FIGURE 3-5. MEMORY EXPANSION OPTION JUMPERS

TABLE 3-2. MEMORY OPTION JUMPER POSITIONS

	OPTION	JUMPER POSITIONS
1.	Memory disabled	E30 to E29
2.	Memory expansion for TM 990/100 or TM 990/101 CPU module	E30 to E32
3.	Memory expansion for 20-bit memory mapping CPU module	E30 to E31

3.3.4 Memory Wait States

In order to properly position the memory wait state jumper, the CPU speed and the access time of the slowest memory device used must be known. Table 3-3 lists the wait states required according to memory access speed and CPU speed. Thus, for known clock and access times for a given system, the number of required wait states can be determined.

As an example, given a CPU clock frequency of 4 MHz and the slowest access time for any of the memory devices is 150 ns: 0 wait states are required and the wait state jumper should be positioned between E21-E22. Table 3-4 shows the jumper positions for different wait state periods.

TABLE 3-3. WAIT STATES

System Clock Frequency	Wait States Required For Specified Memory Access Times			
	0	1	2	3
2 MHz	0-715 ns	.716-1.22 us	1.22-1.72 us	1.72-2.22 us
3 MHz	0-423 ns	424-756 ns	.757-1.09 us	1.09-1.42 us
4 MHz	0-278 ns	279-528 ns	529-778 ns	.779-1.03 us
5 1/3 MHz	0-235 ns	236-423 ns	424-610 ns	611-798 ns

TABLE 3-4. JUMPER POSITIONS FOR DIFFERENT MEMORY WAIT STATES

NUMBER OF MEMORY WAIT STATES	JUMPER POSITIONS
0	E21 to E22
1	E23 to E24
2	E25 to E26
3	E27 to E28

3.3.5 Memory Cycle

The memory cycle early/late jumper should be in the early position (E131 to E132) when either the TM 990/100 or TM 990/101 CPU module is used. The late position is provided for future expansion.

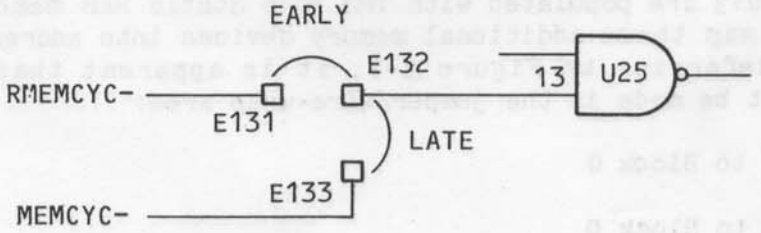


FIGURE 3-6. MEMORY CYCLE JUMPER CONNECTIONS

3.4 MEMORY MAP CONFIGURATION

As stated in Section 3.3.2, a jumper/wire-wrap area is provided in the memory expansion area to allow for easy configuration of the memory map. This configuration system provides the user with universal memory-mapping capability.

In order to configure the memory map so that the additional memory on the TM 990/305 module is mapped into the available memory address space of the CPU module, the appropriate jumper/wire-wrap connections must be made correctly. These connections link the Page select lines to Memory Block 0-3 select lines.

TMS 2516 EPROMs and TMS 4016 RAMs can be addressed as 4K-byte pages within a 16-bit address range. Table 3-5 lists the memory address page boundaries. TMS 2532 EPROMs can only be addressed on even 8K-byte boundaries. In this case, the two page pins must be connected together to the block pin.

TABLE 3-5. MEMORY ADDRESS BOUNDARIES

PAGE	MEMORY ADDRESSES (HEXADECIMAL)
0	0000-0FFF
1	1000-1FFF
2	2000-2FFF
3	3000-3FFF
4	4000-4FFF
5	5000-5FFF
6	6000-6FFF
7	7000-7FFF
8	8000-8FFF
9	9000-9FFF
A	A000-AFFF
B	B000-BFFF
C	C000-CFFF
D	D000-DFFF
E	E000-EFFF
F	F000-FFFF

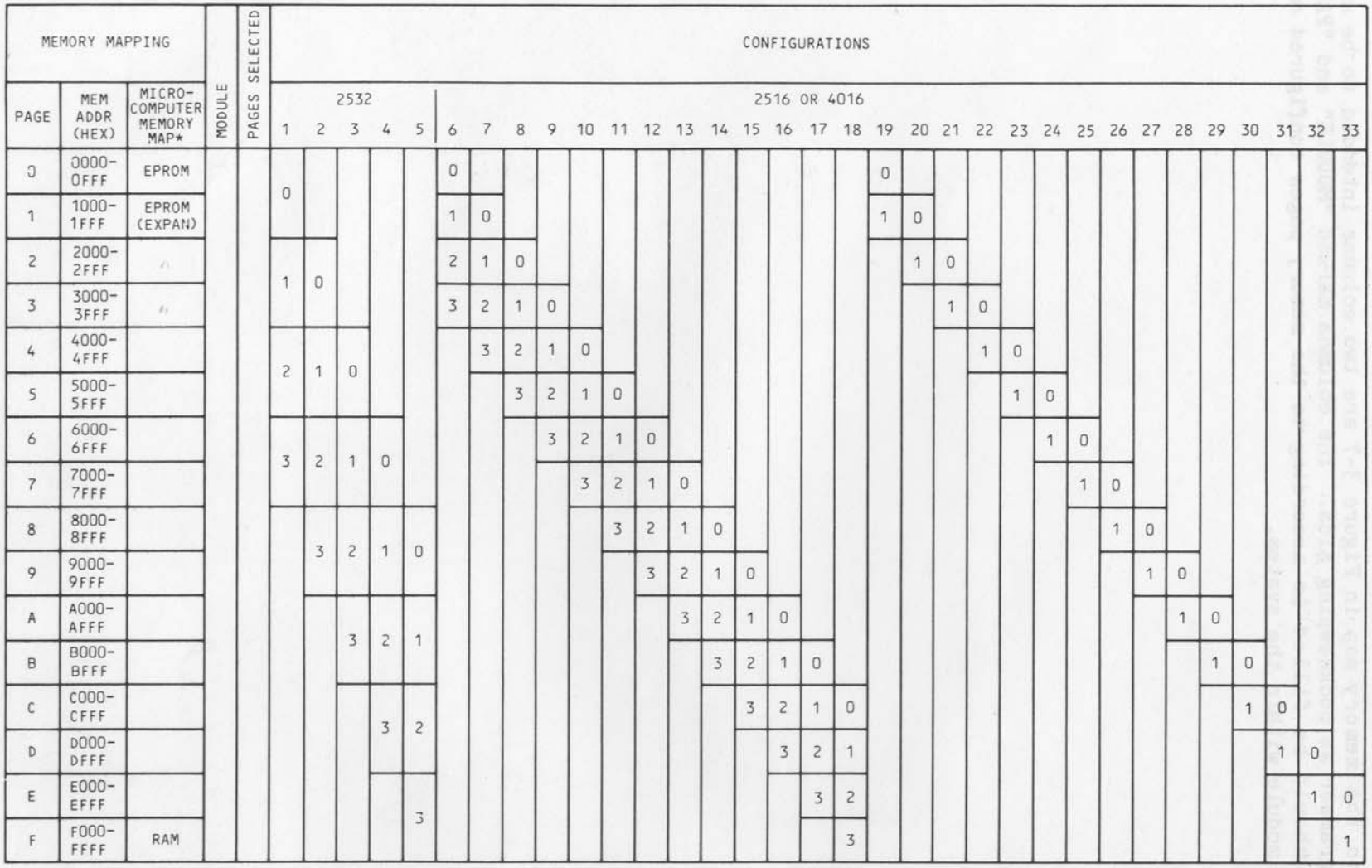
Several suggested memory map configurations are shown in Figure 3-7. Configurations 1-5 are intended for modules populated with TMS 2532 EPROMS, while configurations 6-33 are intended for those modules populated with TMS XX16 memory devices.

As an example, assume that memory sockets U12-U13 are populated with TMS 2532 EPROMs and U14-U19 are populated with TMS 4016 Static RAM memory devices. It is desired to map these additional memory devices into addresses starting at M.A. 2000_{16}. Referring to Figure 3-7, it is apparent that the following connections must be made in the jumper/wire-wrap area:

1. Page 2 to Block 0
2. Page 3 to Block 0
3. Page 4 to Block 1
4. Page 5 to Block 2
5. Page 6 to Block 3.

This configuration would provide additional memory expansion from M.A. 2000_{16} to M. A. $6FFF_{16}$.

Included on the memory map in Figure 3-7 are two columns intended to be used by the programmer as bookkeeping aids. The columns marked "MODULE" and "PAGES SELECTED" should be filled in according to the memory pages configured on a particular module within the system.



*TM 990/100, TM 990/101

NOTE: ENCLOSED NUMBERS 0-3 ABOVE REPRESENT MEMORY BLOCKS

FIGURE 3-7. MEMORY MAP CONFIGURATIONS

SECTION 4

INPUT/OUTPUT PORT CONFIGURATIONS

4.1 GENERAL

The TM 990/305 module provides 16 input channels (Port 1) and 16 individually configurable channels (Port 0) that can be used for input or output. All I/O channels are optically isolated and interface through the Communications Register Unit (CRU).

This section covers the following topics:

- Port 0
- Port 1
- Input/Interrupt Enable
- Interrupt Select
- Interrupt Configuration.

4.2 PORT 0

The 16 channels of Port 0 can be used as inputs or outputs. If a channel is to be used as an output, a 220 ohm 1/2 watt series resistor may be removed to disable the input circuitry. Figure 4-1 shows the circuitry for channel 0 of Port 0. As an example, if it is desired to use channel 0 as an output channel, resistor R48 would be removed to disable the input circuitry on this channel. In this case, reading the channel would always show a logical "ONE". The channel may be used as output with echo-back input by leaving the series resistor in the circuit. In the example of Figure 4-1, the logical state of the line marked INPUT 0 will match that of OUTPUT 0 in this case. It should be noted, however, that the user voltage at the edge connector must be of proper levels to activate the input circuitry for correct echo-back operation. Thus the user should supply a pullup resistor to the signal line giving a voltage between 3.8 and 8.5 volts, referenced to the return line of the channel. If a channel is to be used as an input, it is recommended that the optical isolator in the output circuitry be removed from its socket.

Either a TIL117 or TIL119 optical isolator can be used in an output channel. The TIL117 has an output phototransistor capable of switching between TTL logic levels. The TIL119 has a darlington-connected output phototransistor designed for higher current-carrying capability. Only the TIL117 devices may be used in input channels. Specifications for these two devices can be found in the Optoelectronics Data Book.

4.3 PORT 1

The 16 channels of Port 1 can be used for inputs only. Channels 0 through 3 (Figure 4-2) and channel 15 of this port can be configured as either inputs or interrupts by selecting the proper jumper configuration. Channel 15 can be configured as an input or a board interrupt, i.e., an OR function of masked

interrupts 0-3. Channels 4 through 14 of Port 1 are dedicated input channels.

When configured as interrupts, channels 0 and 2 are <u>negative</u> edge-triggered, while channels 1 and 3 are <u>positive</u> edge-triggered.

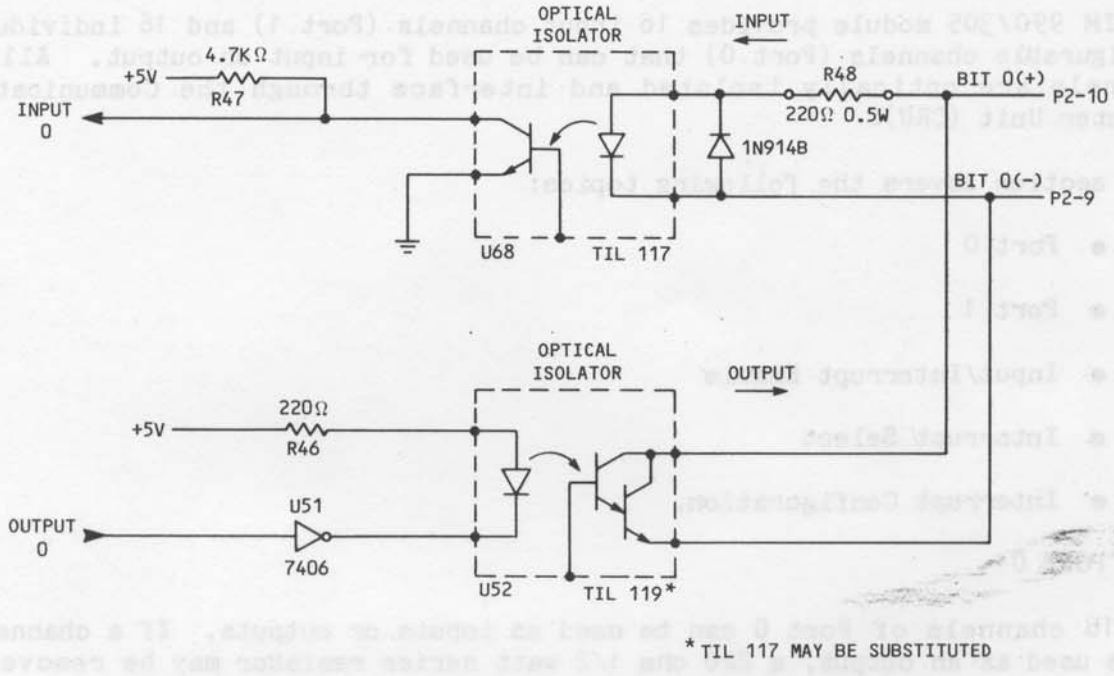


FIGURE 4-1. PORT 0 CIRCUITRY (CHANNEL 0)

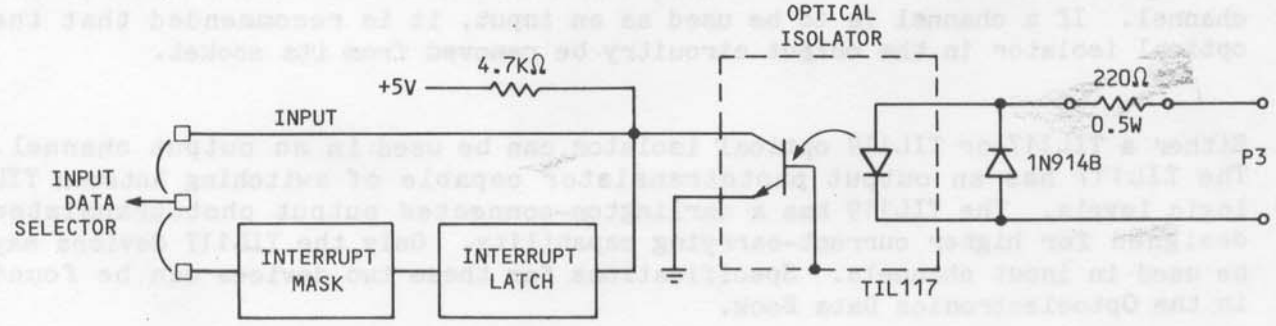


FIGURE 4-2. PORT 1 CIRCUITRY (CHANNELS 0-3)

4.3.1 Input/Interrupt Enable

Table 4-1 shows the jumper connections necessary to configure channels 0 through 3 and channel 15 of Port 1 for either input or interrupt service.

TABLE 4-1. INPUT/INTERRUPT ENABLE JUMPERS

CHANNEL	INPUT ENABLE	INTERRUPT ENABLE
0	E94 to E95	E94 to E93
1	E91 to E92	E91 to E90
2	E88 to E89	E88 to E87
3	E85 to E86	E85 to E84
15	E82 to E83	E82 to E81 Board Interrupt

4.3.2 Interrupt Select

After a channel has been enabled as an interrupt, it is necessary to prioritize or select the desired CPU interrupt level for that channel. Table 4-2 shows the required jumper connections to connect the interrupt source(s) to the chassis backplane where it is monitored by the CPU (via a TMS 9901).

4.3.3 Interrupt Configuration

The TM 990/305 module is shipped with all input/interrupt enable jumpers in the input enable mode. Refer to Tables 4-1 and 4-2 for any interrupt jumper connections desired.

TABLE 4-2. INTERRUPT SELECT JUMPERS

INTERRUPT	SOURCE	CPU INTERRUPT LEVELS
0	E16	
1	E17	E1-E15 Levels 1-15
2	E18	Respectively
3	E19	
Board Interrupt	E20, E134*	

*Electrically connected

SECTION 5

I/O AND INTERRUPT PROGRAMMING

5.1 GENERAL

This section describes how to use the Communications Register Unit (CRU) to do the following:

- Read 1 to 16 input bits (+ and - pairs) at Port 0
- Enable 1 to 16 output bits (+ and - pairs) at Port 0
- Read 1 to 16 input bits (+ and - pairs) at Port 1
- Reset interrupts INT0 to INT3
- Execute a board interrupt reset
- Execute a board reset
- Turn on and turn off LEDs 1 and 2.

It is assumed that the reader is familiar with the various jumper configurations as explained in the tables in Section 2.

5.2 I/O PORTS AT EDGE CONNECTORS P2 AND P3

Thirty-two of the 40 pins at edge connectors P2 (left side of board as viewed in Figure 5-1) and P3 (right side) are programmable through the CRU for I/O and interrupt polling. In software terms, the 32 programmable pins at edge connector P2 are addressable as Port 0 (input or output), and the corresponding 32 pins at P3 are addressable as Port 1 (input only). As shown in Figure 5-1, edge connector pins 1 to 8 are reserved for voltages while pin pairs 9/10 to 39/40 comprise the corresponding 16 programmable bits of Port 0 and Port 1. Table 5-1 lists the pin designations for edge connectors P2 and P3.

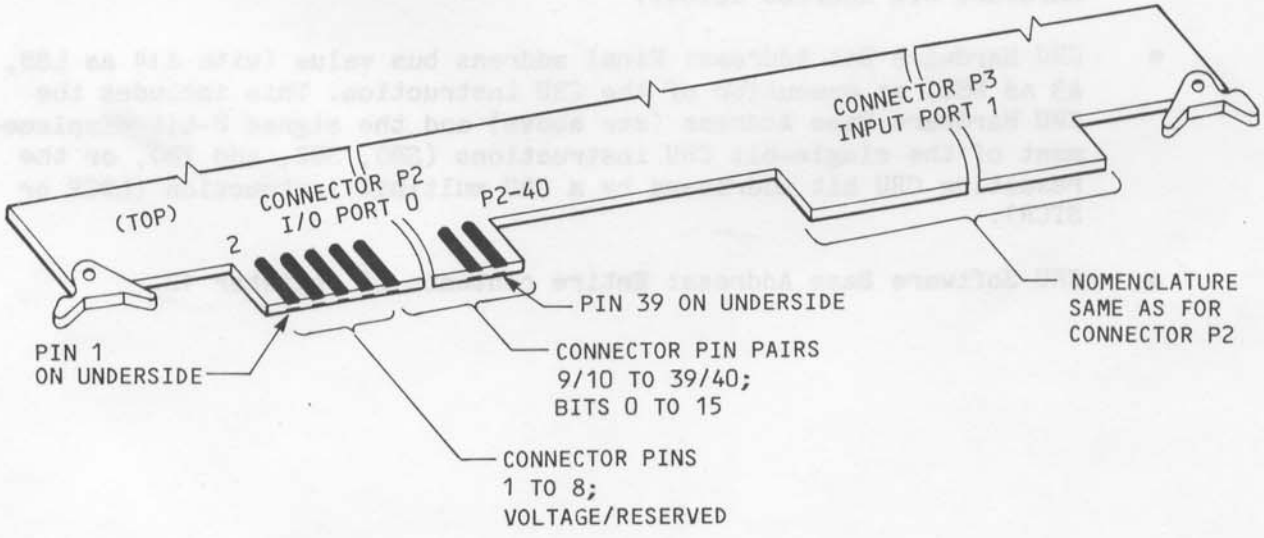


FIGURE 5-1. I/O PORTS AT EDGE CONNECTORS P2 AND P3

TABLE 5-1. EDGE CONNECTOR (P2 AND P3) PIN ASSIGNMENTS

Pin	Signal	Pin	Signal
1	RESERVED	2	RESERVED
3	+5V	4	+8V*
5	GROUND	6	RESERVED
7	GROUND	8	RESERVED
9	BIT 0 (-)	10	BIT 0 (+)
11	BIT 1 (-)	12	BIT 1 (+)
13	BIT 2 (-)	14	BIT 2 (+)
15	BIT 3 (-)	16	BIT 3 (+)
17	BIT 4 (-)	18	BIT 4 (+)
19	BIT 5 (-)	20	BIT 5 (+)
21	BIT 6 (-)	22	BIT 6 (+)
23	BIT 7 (-)	24	BIT 7 (+)
25	BIT 8 (-)	26	BIT 8 (+)
27	BIT 9 (-)	28	BIT 9 (+)
29	BIT 10 (-)	30	BIT 10 (+)
31	BIT 11 (-)	32	BIT 11 (+)
33	BIT 12 (-)	34	BIT 12 (+)
35	BIT 13 (-)	36	BIT 13 (+)
37	BIT 14 (-)	38	BIT 14 (+)
39	BIT 15 (-)	40	BIT 15 (+)

*Edge connector P2 only

5.3 CRU BASE ADDRESS NOMENCLATURE

The following are definitions of CRU address nomenclature. These are shown in Figure 5-2.

- CRU Hardware Base Address: Bits 3 through 14 of register 12 with bits 0 through 2 and 15 being zeros. Bits 3 through 14 of R12 are applied to address bits A3 to A14 (plus signed displacement -- see Hardware Bit Address below).

- CRU Hardware Bit Address: Final address bus value (with A14 as LSB, A3 as MSB) at execution of the CRU instruction. This includes the CRU Hardware Base Address (see above) and the signed 8-bit displacement of the single-bit CRU instructions (SBO, SBZ, and TB), or the resulting CRU bit addressed by a CRU multibit instruction (LDCR or STCR).

- CRU Software Base Address: Entire contents of register 12.

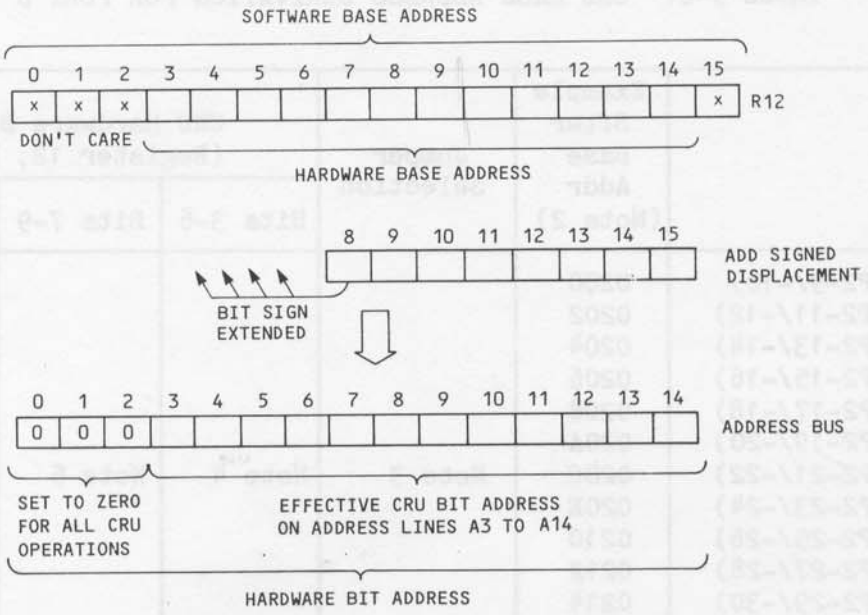


FIGURE 5-2. CRU ADDRESSING NOMENCLATURE

5.4 SELECTING MOST SIGNIFICANT BITS OF CRU HARDWARE BASE ADDRESS

Tables 5-2, 5-3 and 5-4 list the CRU functions on the TM 990/305 module, an example software base address for each (used with the example software and S2 and S1 settings in this section), and the corresponding CRU bit address on address lines A3 to A14 (also corresponding to register 12 bits 3 to 14). Table 5-2 shows Port 0 addressing. Table 5-3 shows Port 1 addressing and necessary jumpers. Table 5-4 shows addressing and jumpers for auxiliary CRU functions. Note that these latter functions use the same addresses as for Port 1 input bits; however, the jumpers are different as shown in Tables 5-3 and 5-4. A complete listing of the CRU functions can be found in Table 6-6 which shows the TM 990/305 CRU map.

There are 32 CRU addressable bits on the TM 990/305 module. These bits are selected via address lines A10 through A14 (five LSBs of the hardware base address) as shown in Tables 5-2 to 5-4. The seven MSBs of the hardware base address are compared to the settings of DIPs S2 (switches 1 through 4 for A3 to A6) and S1 (switches 1 through 3 for A7 through A9). Only CRU instructions with CRU hardware base addresses having the seven MSB's (address line values A3 through A9) corresponding to the two switch settings will be executed on the particular module. This allows using several TM 990/305 modules in a system, each addressable through unique switch-selectable CRU addresses.

To determine the correct S2 and S1 switch settings, first select the desired CRU Hardware Base Address. Address bits 3 to 9 must correspond to the settings of S2 and S1. After selecting the address, set S2 to the values of CRU Hardware Base Address bits 3 to 6 (S2 switches 1 to 4 respectively) and set S1 to the values of CRU Hardware Address bits 7 to 9 (S1 switches 1 to 3 respectively).

NOTE

Switch 4 of S1 is a "don't care" - it is permanently tied to ground and does not correspond to bit 10 of the CRU Hardware Base Address. As shown in Tables 5-2 to 5-4, bit 10 is designated by software.

TABLE 5-2. CRU BASE ADDRESS DERIVATION FOR PORT 0 I/O

Function	Example Sftwr Base Addr (Note 2)	Jumper Selection	CRU Hardware Bit Address[1] (Register 12, Bits 3-14)									
			Bits 3-6	Bits 7-9	10	11	12	13	14			
Port 0 Bit 0 (P2-9/-10)	0200				0	0	0	0	0			
Port 0 Bit 1 (P2-11/-12)	0202				0	0	0	0	1			
Port 0 Bit 2 (P2-13/-14)	0204				0	0	0	1	0			
Port 0 Bit 3 (P2-15/-16)	0206				0	0	0	1	1			
Port 0 Bit 4 (P2-17/-18)	0208				0	0	1	0	0			
Port 0 Bit 5 (P2-19/-20)	020A				0	0	1	0	1			
Port 0 Bit 6 (P2-21/-22)	020C	Note 3	Note 4	Note 5	0	0	1	1	0			
Port 0 Bit 7 (P2-23/-24)	020E				0	0	1	1	1			
Port 0 Bit 8 (P2-25/-26)	0210				0	1	0	0	0			
Port 0 Bit 9 (P2-27/-28)	0212				0	1	0	0	1			
Port 0 Bit 10 (P2-29/-30)	0214				0	1	0	1	0			
Port 0 Bit 11 (P2-31/-32)	0216				0	1	0	1	1			
Port 0 Bit 12 (P2-33/-34)	0218				0	1	1	0	0			
Port 0 Bit 13 (P2-35/-36)	021A				0	1	1	0	1			
Port 0 Bit 14 (P2-37/-38)	021C				0	1	1	1	0			
Port 0 Bit 15 (P2-39/-40)	021E				0	1	1	1	1			

NOTES:

1. When displacement is zero, each R12 bit 3 to 14 is equal to the same numbered address line (A3 to A14) and R12 bits 3 to 14 are equal to the hardware bit address.

2. The examples in this section use a CRU hardware base address of 0100_{16} (software base address of 0200_{16}). The middle two hex values of the hardware base address must be set (for comparison) in DIPs S2 and S1. Thus, for these examples DIP S2 is set to 0001_2 (ON-ON-ON-OFF) and DIP S1 is set to 0000_2 (all ON). See notes 4 and 5.

3. Port 0 functions are not jumper selectable.

4. R12 bits 3 to 6 correspond to S2 settings (0001_2). See note 2.

5. R12 bits 7 to 9 correspond to S1 settings, switches 1 to 3 (000_2). Switch 4 is a "don't care" and is hard-wired to ground (thus does not represent bit 10 of R12). See note 2.

TABLE 5-3. CRU BASE ADDRESS DERIVATION FOR PORT 1 INPUTS

Function	Example Sftwr Base Addr (Note 2)	Jumper Selection	CRU Hardware Bit Address[1] (Register 12, Bits 3-14)						
			Bits 3-6	Bits 7-9	10	11	12	13	14
Port 1 Bit 0 (P3-9/-10)	0220	E94-E95			1	0	0	0	0
Port 1 Bit 1 (P3-11/-12)	0222	E91-E92			1	0	0	0	1
Port 1 Bit 2 (P3-13/-14)	0224	E88-E89			1	0	0	1	0
Port 1 Bit 3 (P3-15/-16)	0226	E85-E86			1	0	0	1	1
Port 1 Bit 4 (P3-17/-18)	0228				1	0	1	0	0
Port 1 Bit 5 (P3-19/-20)	022A				1	0	1	0	1
Port 1 Bit 6 (P3-21/-22)	022C		Note 3	Note 4	1	0	1	1	0
Port 1 Bit 7 (P3-23/-24)	022E				1	0	1	1	1
Port 1 Bit 8 (P3-25/-26)	0230				1	1	0	0	0
Port 1 Bit 9 (P3-27/-28)	0232				1	1	0	0	1
Port 1 Bit 10 (P3-29/-30)	0234				1	1	0	1	0
Port 1 Bit 11 (P3-31/-32)	0236				1	1	0	1	1
Port 1 Bit 12 (P3-33/-34)	0238				1	1	1	0	0
Port 1 Bit 13 (P3-35/-36)	023A				1	1	1	0	1
Port 1 Bit 14 (P3-37/-38)	023C				1	1	1	1	0
Port 1 Bit 15 (P3-39/-40)	023E	E82-E83			1	1	1	1	1

NOTES:

1. When displacement is zero, each R12 bit 3 to 14 is equal to the same numbered address line (A3 to A14) and R12 bits 3 to 14 are equal to the hardware bit address.

2. The examples in this section use a CRU hardware base address of 0100_{16} (software base address of 0200_{16}). The middle two hex values of the hardware base address must be set (for comparison) in DIPs S2 and S1. Thus, for these examples DIP S2 is set to 0001_2 (ON-ON-ON-OFF) and DIP S1 is set to 0000_2 (all ON). See Notes 3 and 4.

3. R12 bits 3 to 6 correspond to S2 settings (0001_2). See Note 2.

4. R12 bits 7 to 9 correspond to S1 settings, switches 1 to 3 (000_2). Switch 4 is a "don't care" and is hard-wired to ground (thus does not represent bit 10 of R12). See Note 2.

TABLE 5-4. CRU BASE ADDRESS DERIVATION FOR AUXILIARY FUNCTIONS

Function	Example Sftwr Base Addr (Note 2)	Jumper Selection	CRU Hardware Bit Address[1] (Register 12, Bits 3-14)									
			Bits 3-6	Bits 7-9	10	11	12	13	14			
Reset/Poll INT0-(P3-9/-10)	0220	E94-E93			1	0	0	0	0			
Reset/Poll INT1-(P3-11/-12)	0222	E91-E90			1	0	0	0	1			
Reset/Poll INT2-(P3-13/-14)	0224	E88-E87			1	0	0	1	0			
Reset/Poll INT3-(P3-15/-16)	0226	E85-E84			1	0	0	1	1			
			Note 3	Note 4								
MASK/UNMASK INT0-	0230				1	1	0	0	0			
MASK/UNMASK INT1-	0232				1	1	0	0	1			
MASK/UNMASK INT2-	0234				1	1	0	1	0			
MASK/UNMASK INT3-	0236				1	1	0	1	1			
ON/OFF LED 1 (Note 5)	0238				1	1	1	0	0			
ON/OFF LED 2 (Note 5)	023A				1	1	1	0	1			
BOARD RESET (Note 6)	023C				1	1	1	1	0			
BOARD INTERRUPT7(P3-39/-40)	023E	E82-E81			1	1	1	1	1			

NOTES:

1. When the displacement is zero, R12 bits 3 to 14 correspond to the same numbered address line (A3 to A14) and R12 bits 3 to 14 are equal to the hardware bit addres

2. The examples in this section use a CRU hardware base address of 0100_{16} (software base address of 0200_{16}). The middle two hex values of the hardware base address must be set (for comparison) in DIPS - S2 and S1. Thus, for these examples, DIP S2 is set to 0001_2 (ON-ON-ON-OFF) and DIP S1 is set to 0000_2 (all ON). See notes 3 and 4.

3. R12 bits 3 to 6 correspond to S2 settings (0001_2). See Note 2.

4. R12 bits 7 to 9 correspond to S1 settings, switches 1 to 3 (000_2). Switch 4 is a "don't care" and is hard-wired to ground (thus does not represent bit 10 of R12. See Note 2.

5. Writing a one to the LED CRU bit address lights the LED; writing a zero turns off the LED.

6. Writing a one or zero to the Board Reset CRU bit address resets the board as follows:

   - Port 0 outputs at low levels (outputs open)
   - Interrupt latches to "no interrupt" status
   - Interrupt masks to "interrupt disabled" status

7. When jumpered, any of the enabled four interrupts will cause a board interrupt to be read at this CRU address. A one indicates an enabled (mask enabled) interrupt request is active. Resetting all enabled interrupts results in a zero at this address.

5.5 CONSIDERATIONS

5.5.1 Configure Port 0 Interfaces for Either Input or Output

Figure 5-3 is a schematic of the opto-coupler interface at Port 0. Port 1 is similar except it does not contain the output circuit at the bottom of the figure. Thus, each interface at Port 0 can be configured as either an input or an output (or both) while all interfaces at Port 1 can be used for input only. The user may designate each interface at Port 0 as an input or an output by one of the following methods:

- Pull out the output opto-coupler (U52 to U67) and install the input series resistor (R48 to R63) to create an input interface, or
- Pull out the input series resistor (R48 to R63) and install the output opto-coupler (U52 to U67) to create an output interface.
- Leave the output opto-coupler and input series resistor installed for echo-back (input) output operation.

5.5.2 Enable Output Bit

To enable an output bit at Port 0 (Port 1 is input only), write a one to the appropriate bit. This causes the opto-coupler output to be closed, completing the circuit to the edge-connector pair.

5.5.3 Disable Output Bit

To disable an output bit, write a zero to the bit. This causes the opto-coupler output to be open, breaking the circuit to the edge-connector pair.

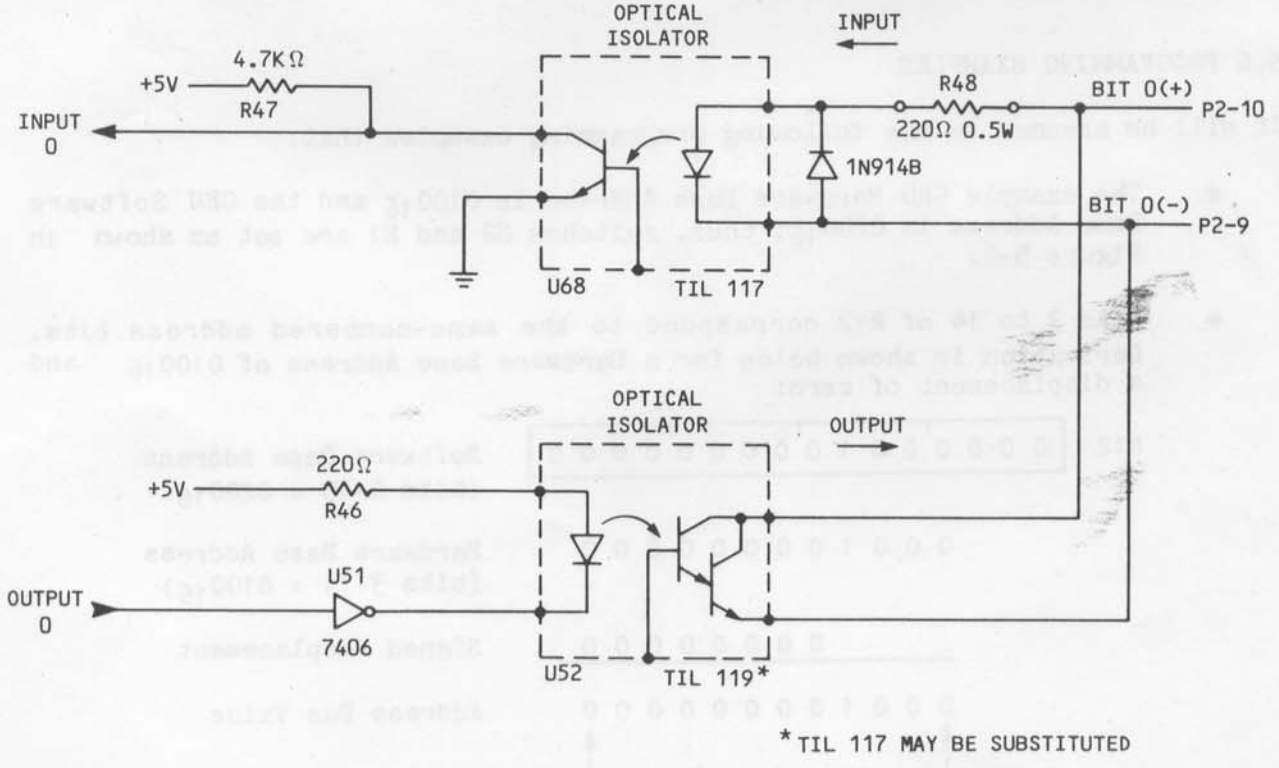


FIGURE 5-3. EDGE CONNECTOR OPTO-COUPLER INTERFACE

5.5.4 Read Input Bit

To determine the status of an input bit, the following apply:

- If the opto-coupler at an input bit is enabled (output closed), a zero will be read at the input bit. For example:

```
LI   R12,CRUADR      INPUT BIT SFTWR BASE ADDR
TB   0               TEST BIT
JNE  ENABLD          ZERO = ENABLED
       •
       •
       •
```

  If the opto-coupler is enabled (presumably by an off-board high-level signal applied), a zero will be sensed on board and the jump-if-not-equal will be executed.

- If the opto-coupler at the input bit is disabled (opto-coupler output open), a one will be read at the input bit. For example:

```
LI   R12,CRUADR      INPUT BIT SFTWR BASE ADDR
TB   0               TEST BIT
JEQ  DISABL          ONE = DISABLED
       •
       •
       •
```

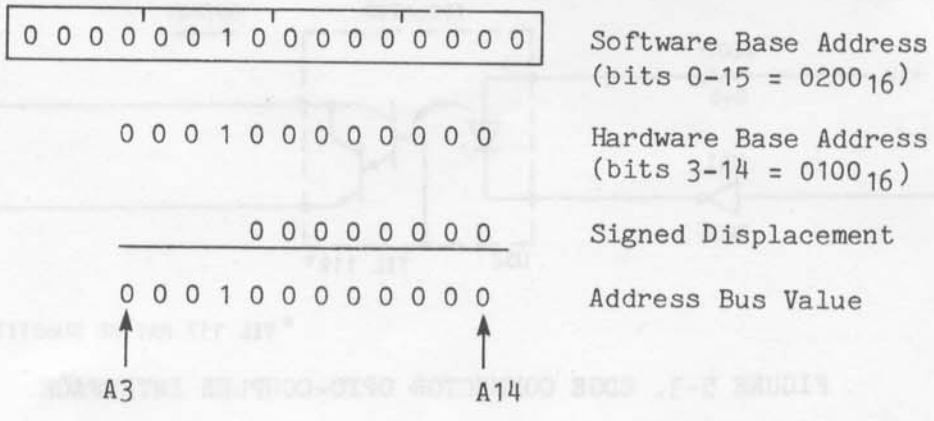
  If the opto-coupler is disabled (presumably by an off-board low-level signal applied), a one will be sensed onboard and the jump-if-equal will execute.

5.6 PROGRAMMING EXAMPLES

It will be assumed in the following programming examples that:

- The example CRU Hardware Base Address is 0100_{16} and the CRU Software Base Address is 0200_{16}; thus, switches S2 and S1 are set as shown in Figure 5-4.

- Bits 3 to 14 of R12 correspond to the same-numbered address bits. Derivation is shown below for a Hardware Base Address of 0100_{16} and a displacement of zero:



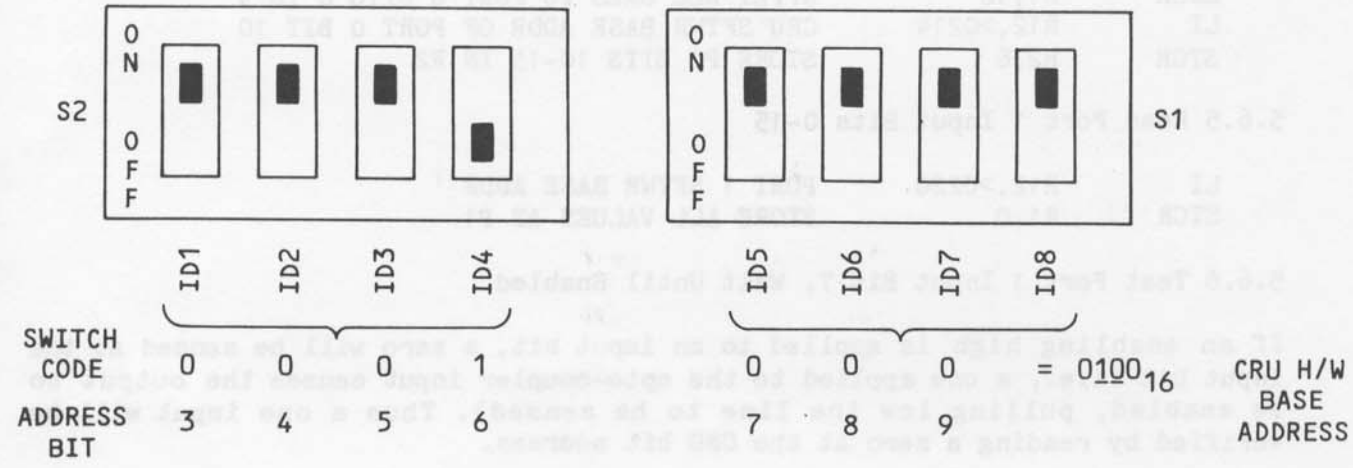


FIGURE 5-4. SETTINGS OF SWITCHES S2 AND S1 FOR PROGRAMMING EXAMPLES

IMPORTANT NOTE

Since opto-isolator circuits take tens of microseconds to switch, it is possible for the processor to outrace the devices and read erroneous values while the addressed devices are switching. All software must take this fact into account, and delay loops or repeated testing of the desired I/O line may have to be used in certain programming situations.

5.6.1 Write a One to Port 0 Output Bit 0

```
LI      R12,>0200       CRU SFTWR BASE ADDR OF PORT 0 BIT 0
SBO     0               SET P0 BIT 0 TO ONE
```

This causes the output side of the opto-coupler at Port 0 bit 0 to close.

5.6.2 Input (Store) a Bit from Port 0 Input Bit 0

```
CLR     R1              CLEAR STORAGE AREA
LI      R12,>0200       CRU SFTWR BASE ADDR OF PORT 0 BIT 0
STCR    R1,1            STORE PORT 0 BIT 0 VALUE IN R1
```

5.6.3 Write All Ones to Port 0 Output Bits 0-6

```
LI      R1,>7F00        SET ONES VALUE IN R1 LEFT BYTE
LI      R12,>0200       CRU SFTWR BASE ADDR OF PORT 0
LDCR    R1,7            APPLY ONES TO PORT 0 BITS 0 TO 6
```

5.6.4 Write All Ones to Port 0 Output Bits 0-9, Read Values at Port 0 Input Bits 10-15

```
LI      R1,>03FF      SET 10 ONES VALUE IN R1
CLR     R2            CLEAR STORAGE REGISTER
LI      R12,>0200     CRU SFTWR BASE ADDR
LDCR    R1,10         APPLY ALL ONES TO PORT 0 BITS 0 TO 9
LI      R12,>0214     CRU SFTWR BASE ADDR OF PORT 0 BIT 10
STCR    R2,6          STORE P0 BITS 10-15 IN R2
```

5.6.5 Read Port 1 Input Bits 0-15

```
LI      R12,>0220     PORT 1 SFTWR BASE ADDR
STCR    R1,0          STORE ALL VALUES AT P1
```

5.6.6 Test Port 1 Input Bit 7, Wait Until Enabled

If an enabling high is applied to an input bit, a zero will be sensed at the input bit (i.e., a one applied to the opto-coupler input causes the output to be enabled, pulling low the line to be sensed). Thus a one input will be verified by reading a zero at the CRU bit address.

```
      LI   R12,>0220     SET SFTWR BASE ADDR FOR PORT 1
WAIT  TB   7             BIT 7 ENABLED?
      JEQ  WAIT          NO, ONE FOUND (HIGH FOUND), LOOP BACK
       •                 YES, ZERO FOUND, CONTINUE
       •
       •
```

5.6.7 Interrupts

Port 1 input bits 0 to 3 will contain interrupt inputs (INT0 to INT3) if jumpered accordingly. A one level indicates an interrupt and a zero indicates no interrupt.

Interrupts INT0 and INT2 are negative edge-triggered, meaning a transition from a high level to a low level at the external input will cause an interrupt indication. Interrupts INT1 and INT3 are positive-going and require a transition from a low to a high state.

Interrupts can be sensed in the following ways:

1) Poll the interrupt via CRU addresses since the interrupt (if jumpered) will set a latch which can be tested (and also reset) through the CRU.

2) If jumpered for board interrupt (jumper E81-82), a one read at the CRU address for Port 1 bit 15 indicates that at least one of the four interrupts has become active, and polling could be used to further determine which interrupt(s) is enabled. This bit will remain a one as long as all enabled interrupt requests remain active; when these requests are reset, this bit goes to a zero.

3) If additional jumpering is made at the interrupt wire-wrap area, the interrupt (INT0 to INT3 and board interrupt) will also be routed via

backplane edge connector P1 to the system bus interrupt lines. A low logic level will be issued when an interrupt is active. Figure 5-5 shows the interrupt jumper area in the lower left of the TM 990/305 module. The center pins I0, I1, I2, and I3 (corresponding to interrupts 0 to 3) and BI (board interrupt) can be routed to interrupt levels 1 to 15 (outer rows of pins) at the microcomputer board TMS 9901.

Each of the four interrupts can be enabled by setting the respective interrupt mask bit to a one. Writing a zero to the mask bit disables the interrupt. Interrupt mask CRU addresses are listed in Table 5-4. The interrupt mask must be enabled before the interrupt can be sensed through the CRU or sent to the system bus. Enabled interrupts are also routed to jumper pins E16 to E20 for jumpering to the desired system bus interrupt level as described in 3) above.

All interrupts can be individually reset by writing either a one or zero to the interrupt CRU address. Writing to the board interrupt reset (CRU software base address $023E_{16}$) will reset all interrupts and interrupt masks, and open the outputs of Port 0. CRU addresses for these functions are listed in Table 5-4.

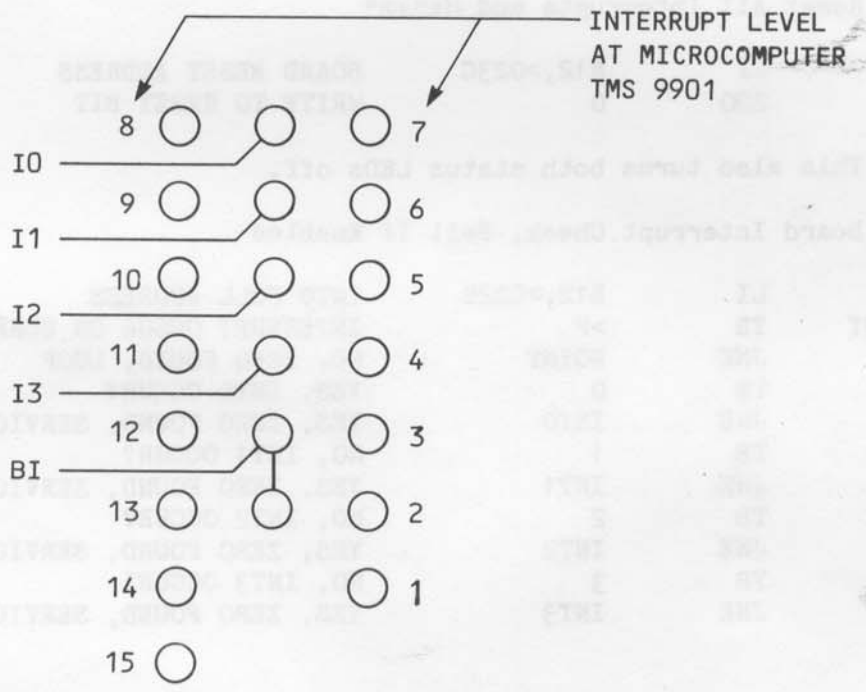


FIGURE 5-5. INTERRUPT JUMPER/WIRE-WRAP AREA

5.6.7.1 Enable INT0, Wait for Interrupt

```
        LI      R12,>0230       INT0 MASK ADDRESS
        SBO     0               ENABLE MASK
NOINT   TB      -8              INT0 ACTIVE?
        JEQ     NOINT           JUMP UNTIL INT ACTIVE
          •
          •
          •
```

5.6.7.2 Enable INT0, INT1 Masks; Disable INT2, INT3 Masks

```
        LI      R12,>0230       INT0 MASK ADDRESS
        LI      R1,>0300        BITS TO ENABLE MASKS
        LDCR    R1,4            ENABLE MASKS
```

Logical ones will be output to enable INT0 and INT1; logical zeroes will be output to disable INT2 and INT3.

5.6.7.3 Reset All Interrupts

```
        LI      R12,>0220       INT0 RESET ADDRESS
        LI      R1,>0F00        BITS TO RESET ALL FOUR INTERRUPTS
        LDCR    R1,4            RESET ALL INTERRUPTS
```

5.6.7.4 Reset All Interrupts and Masks*

```
        LI      R12,>023C       BOARD RESET ADDRESS
        SBO     0               WRITE TO RESET BIT
```

* This also turns both status LEDs off.

5.6.7.5 Board Interrupt Check, Poll If Enabled

```
        LI      R12,>0220       INT0 POLL ADDRESS
NOINT   TB      >F              INTERRUPT OCCUR ON BOARD?
        JNE     NOINT           NO, ZERO FOUND, LOOP
        TB      0               YES, INT0 OCCUR?
        JNE     INT0            YES, ZERO FOUND, SERVICE INT0
        TB      1               NO, INT1 OCCUR?
        JNE     INT1            YES, ZERO FOUND, SERVICE INT1
        TB      2               NO, INT2 OCCUR?
        JNE     INT2            YES, ZERO FOUND, SERVICE INT2
        TB      3               NO, INT3 OCCUR?
        JNE     INT3            YES, ZERO FOUND, SERVICE INT3
```

5.6.8 Reset Board

Writing to the board reset CRU bit does the following:

- Resets all Port 0 outputs to an open state
- Resets all latched interrupts to "no-interrupt" status
- Resets all interrupt masks to "disable interrupt" level.

```
        LI      R12,>023E       BRD RESET CRU ADDRESS
        SBO     0               ISSUE BOARD RESET
```

- Turns both status LEDs off.

NOTE

Any CRU write instruction (SBO, SBZ, or LDCR) to the board reset CRU bit address will cause a board reset.

5.6.9 LEDs DS1 and DS2

5.6.9.1 Turn On and Off LEDs DS1 and DS2. Two LEDs, DS1 and DS2 are located near the edge of the board between Port 0 and Port 1. These LEDs can be turned on or turned off by writing, respectively, a one (turn on) or a zero (turn off) to their CRU addresses.

```
        LI      R12,>0238       DS1 CRU SFTWR BASE ADDR
        SBO     0               TURN ON DS1
        SBO     1               TURN ON DS2
         •
         •
         •
        CLR     R1              R1 TO ALL ZEROES
        LDCR    R1,2            TURN OFF LEDS (ZERO TO BOTH)
```

5.6.9.2 Blink LED Program. The following software alternately turns one LED on and the other off at one-second intervals.

```
        LI      R12,>0238       DS1 CRU SFTWR BASE ADDR
        LI      R1,37500        LOOP1 COUNT FOR 250 MS
        LI      R3,>0102        LIGHT BIT PATTERN
LOOP0   LI      R4,4            DO LOOP1 4 TIMES
        SWPB    R3              BRING UP NEW ON/OFF PATTERN
        LDCR    R3,2            ON/OFF LED'S
LOOP1   MOV     R1,R2           MOVE LOOP1 COUNT TO R2
LOOP2   DEC     R2              DECREMENT R2
        JNE     LOOP2           LOOP UNTIL R2 = 0
        DEC     R4              DECREMENT R4
        JNE     LOOP1           REDO LOOP1/LOOP2 UNTIL R4 = 0
        JMP     LOOP0           1 SEC COMPLETE, REPEAT
```

SECTION 6

THEORY OF OPERATION

6.1 GENERAL

This section describes the theory of operation of the TM 990/305 module. Block diagrams of the memory and control logic (Figure 6-1) and input/output circuitry (Figure 6-2) are provided in this section while the principal components are identified in Figure 1-1. Supplementary information can be found in the following manuals:

- TMS 9900 Microprocessor Data Manual
- The MOS Memory Data Book, 1979 Edition
- The Optoelectronics Data Book.

Data sheets for the TMS 4016 static RAM, TMS 2516 EPROM, and TMS 2532 EPROM are included in Appendices G and H.

6.2 SYSTEM STRUCTURE

The block diagrams in Figures 6-1 and 6-2 show the system structure of the TM 990/305 memory and I/O module. The design centers around four buses: control, address, data, and CRU. The major blocks of the module are RAM/EPROM memory, memory address decoding, CRU address decoding, input/output circuitry, interrupt select logic, and miscellaneous control signals. Functionally these major blocks represent the control, memory, and I/O sections of the module.

6.3 SYSTEM BUSES

Table 6-1 provides a listing of the system bus signals. A description of the signals on the address, data, CRU, and control buses follows.

6.3.1 Address Bus

The address bus consists of lines A0 through A14 and XA0 through XA3. Address lines A0 through A14 are used in a 16-bit address system, such as a TM 990/100 of TM 990/101 based system (Note that bit A15 is always output as a zero on the address bus in these systems). Address lines XA0-XA3 are for extended address bits used only in a 20-bit address system that utilizes a memory-mapping processor.

On the module, lines A0-A3 are decoded by a memory address decoder to yield memory device select lines. Line A3 is also routed to the CRU base address decoder and jumpered to TMS 2532 EPROMs when installed. This leaves lines A4-A14 to address all memory devices on board and control the I/O decode logic. Additional information on memory addressing is contained in Section 6.5.

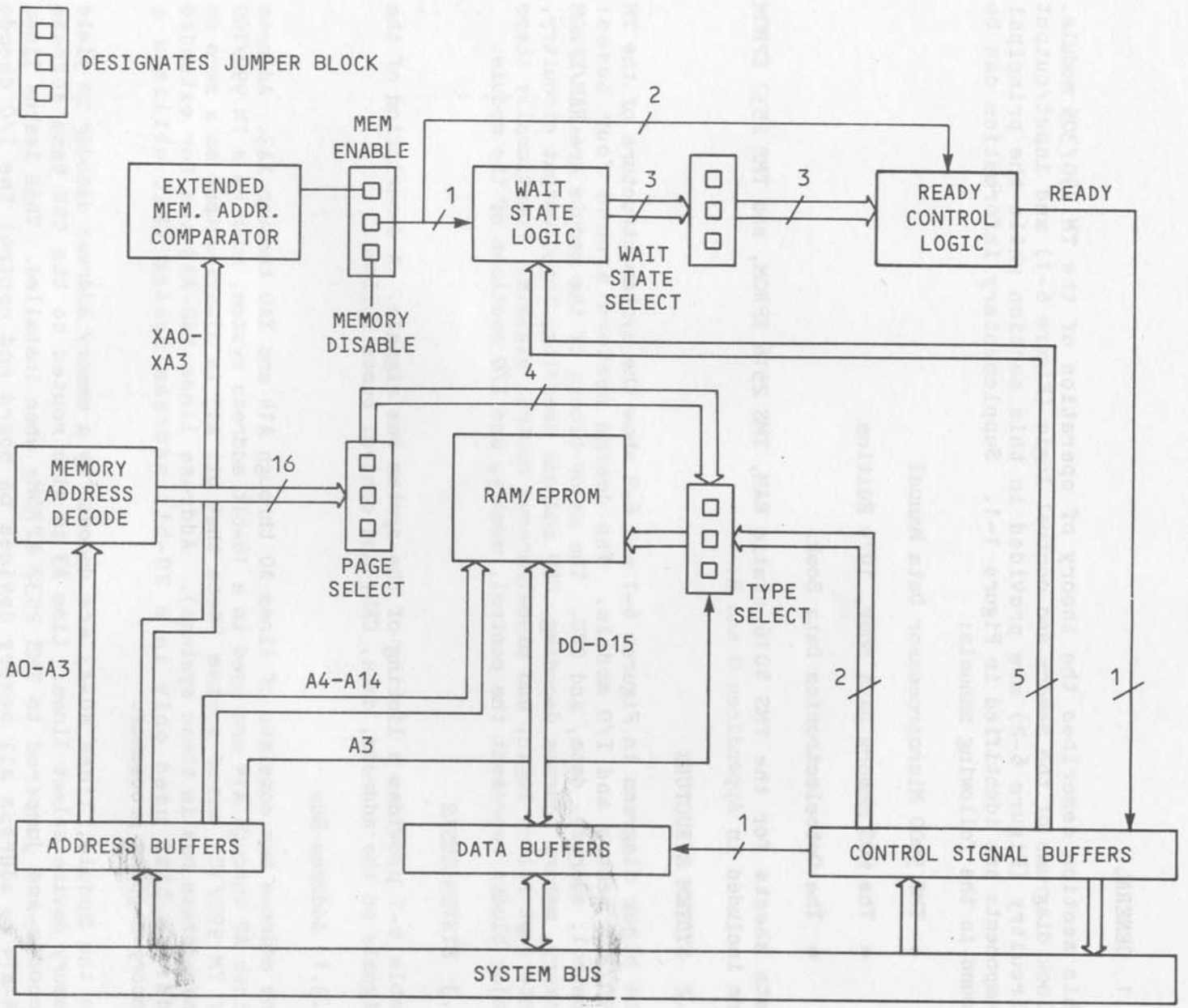


FIGURE 6-1. MEMORY AND CONTROL LOGIC

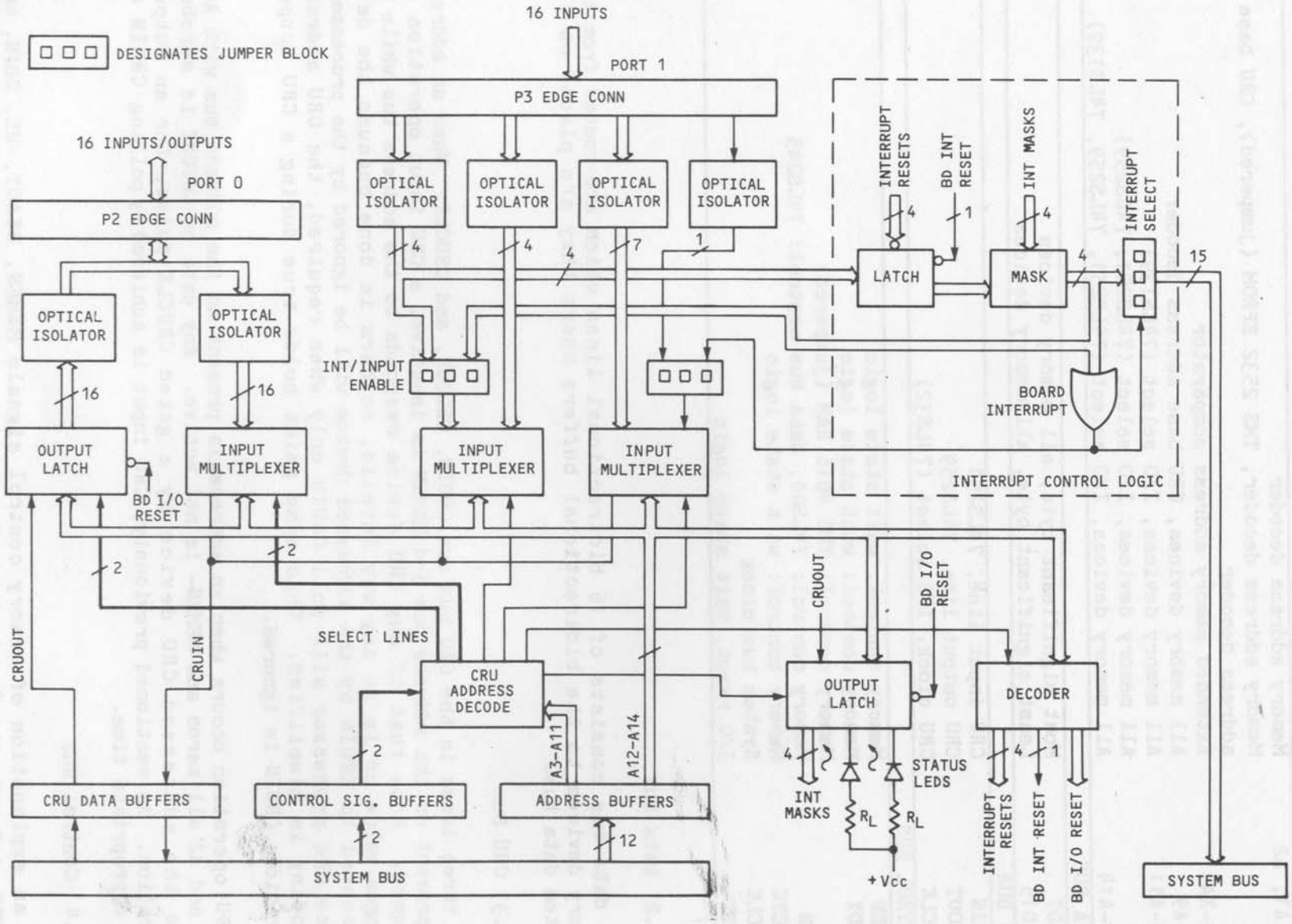


FIGURE 6-2. I/O LOGIC

TABLE 6-1. SYSTEM BUS SIGNALS

SIGNAL	FUNCTIONAL DEVICE CONNECTIONS
ADDRESS BUS	
A0,A1, A2	Memory address decoder
A3	Memory address decoder, TMS 2532 EPROM (jumpered), CRU base address decoder
XA0-XA3	Extended memory address comparator
A4-A9	All memory devices, CRU base address decoder
A10-A11	All memory devices, I/O select (74LS139)
A12	All memory devices, I/O select (74LS251, 74LS259)
A13-A14	All memory devices, I/O select (74LS251, 74LS259, 74LS139)
DATA BUS	
D0-D7	Most significant byte, all memory devices
D8-D15	Least significant byte, all memory devices
CRU BUS	
CRUIN	CRU input line, 74LS251
CRUOUT	CRU output line, 74LS259
CRUCLK	CRU clock, I/O select (74LS32)
CONTROL BUS	
MEMEN	Memory control: wait state logic
READY	Memory control: wait state logic
WE	Memory control: TMS 4016 RAM (jumpered)
DBIN	Memory control: 74LS00, data bus control: 74LS245
MEMCYC	Memory control: wait state logic
BUSCLK	System bus clock
IORST	I/O reset, wait state logic

6.3.2 Data Bus

The data bus consists of 16 bidirectional lines which are routed from the memory devices to the bidirectional buffers where they are placed on the system data bus.

6.3.3 CRU Bus

The three lines in the CRU bus are CRUIN, CRUOUT, and CRUCLK. When an address is present on the address bus and MEMEN is inactive, a CRU input operation is assumed. Note that if any CRU device responds to the address bus while it changes value or is in any way invalid, no harm is done because the data presented to CRUIN by the addressed device will be ignored by the processor. Since the processor will poll CRUIN only when required, the CRU address decoding is simplified. This same point holds true during a CRU output operation: CRUIN is ignored.

A CRU operation occurs when an address is present on the address bus with A0, A1, and A2 all zeros and MEMEN- is not active. Any data on CRUOUT is strobed into the addressed CRU device by a gated CRUCLK pulse, for an output operation. As mentioned previously, CRU input is achieved by polling CRUIN at the appropriate time.

6.3.4 Control Bus

For an explanation of memory control signals MEMEN, READY, WE, DBIN, and MEMCYC, refer to the User's Guide for the processor used in the system.

BUSCLK is the system bus clock, while IORST is the processor-generated I/O reset signal.

6.4 QUICK REFERENCE GUIDE

A quick-reference user's guide is located in the lower right-hand corner of the module. The purpose of the guide is to provide the user with the necessary information, in condensed form, required to reconfigure three basic areas, 1. Memory, 2. I/O Port 0, and 3. Input Port 1. The guide is listed here in Table 6-2 along with the sections explaining the function of each control element.

TABLE 6-2. QUICK REFERENCE GUIDE

	MEMORY		
	STAKE PINS	FUNCTION	SECTIONS
JUMPERS	E33→E56	Type select	3.3.1
JUMPERS	E57→E80	Page select	3.3.2, 3.4, 6.6
JUMPERS	E29→E32	Memory enable	3.3.3, 6.5
JUMPERS	E21→E28	Wait states	3.3.4, 6.7
	E131→E133	Early/late	3.3.5
SW	SWITCHES		
SW	S3	Extended address select	6.5
	I/O PORT 0		
OCI	OPTICAL ISOLATORS	FUNCTION	
OCI	U52→U67	Output	4.2, 5.5.1, 6.10.2
OCI	U68→U83	Input	4.2, 5.5.1, 6.10.1
RES	RESISTORS*		
RES	R48→R63	Input (* Remove for output channels)	4.2, 5.5.1, 6.10.1
SW	SWITCHES		
SW	S1, S2	CRU address select	6.9
	INPUT PORT 1		
OCI	OPTICAL ISOLATORS	FUNCTION	
OCI	U84→U99	Input	4.3, 6.11
RES	RESISTORS		
RES	R64→R79	Input	4.3, 6.11
	STAKE PINS		
JUMPERS	E1→E19	Interrupt Select	4.3.2, 5.6.7, 6.11.1
JUMPERS	E20	Board Interrupt Select	4.3.2, 5.6.7, 6.11.1
JUMPERS	E84→E95	Input/Interrupt Enable	4.3.1, 5.6.7, 6.11.1
JUMPERS	E81→E83	Input/Board Interrupt Enable	4.3.1, 5.6.7, 6.11.1
SW	SWITCHES		
SW	S1, S2	CRU address select	6.9

6.5 MEMORY ADDRESS DECODING

Address lines A0-A3 are decoded by the circuitry shown in Figure 6-3. The memory address decode circuitry generates page select lines 0-F which enable the addressed memory device. The LS145 decoders have open collector outputs and may be connected together when using TMS 2532 EPROMs (See Page Select Example, Section 6.6.1).

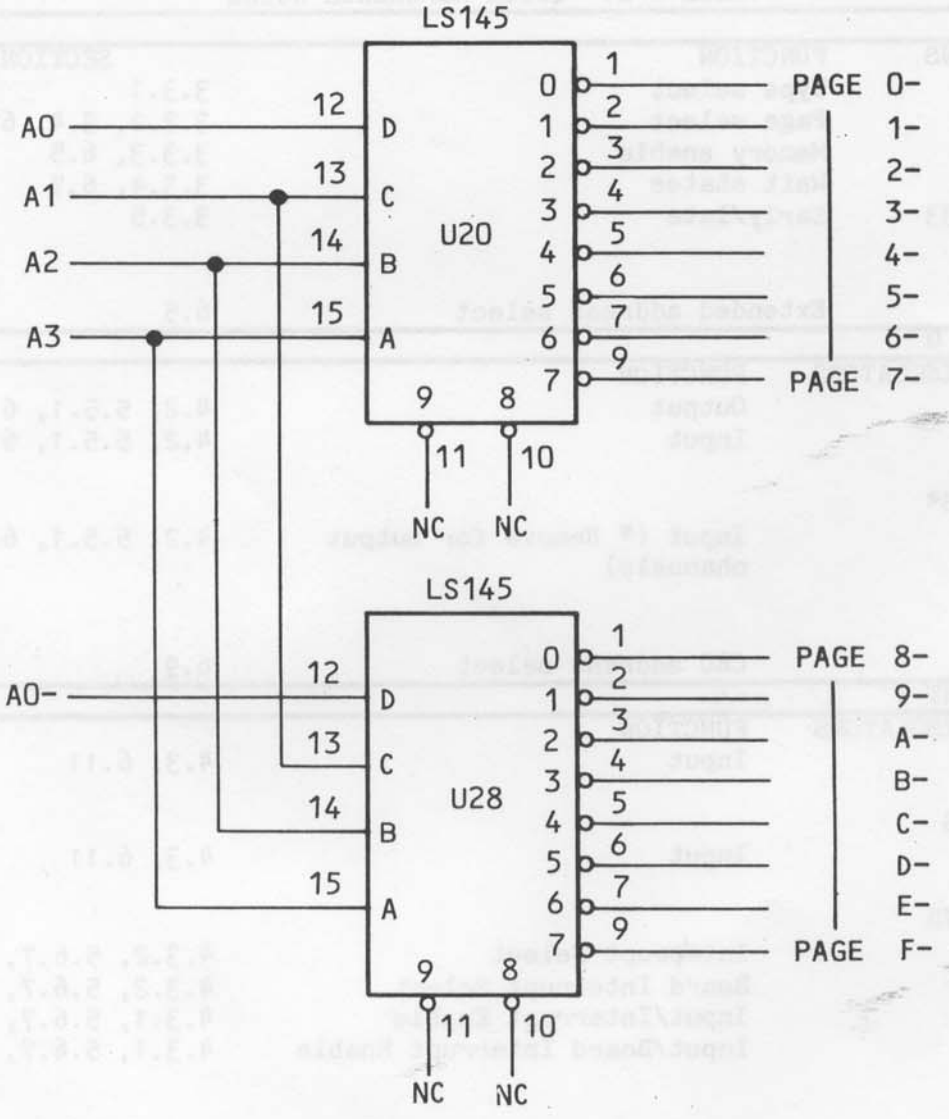


FIGURE 6-3. MEMORY ADDRESS DECODE

When RAM memory in excess of 64K bytes is needed, a processor board with an on-board mapping controller must be used. A 20-bit address is then placed on the system bus. The 20-bit address consists of address bits A0-A15 and extended address bits XA0-XA3, with XA0 as the most significant bit. This allows memory expansion to 1,048,576 bytes of which any sixteen 4K-byte page (or 64K-bytes) can be mapped into the logical memory space at one time.

Decoding of the extended address bits XA0-XA3 is accomplished by comparing the value of the four extended address bits to a DIP-switch (S3) setting (Refer to Figure 6-4.)

When using a mapping controller, stake pins E30 and E31 must be jumpered. When using a TM 990/100 or TM 990/101 processor, stake pins E30 and E32 must be jumpered. To disable <u>all</u> memory on the TM 990/305 module, pins E29 and E30 must be jumpered. If no memory is present, then the jumper must be positioned to disable all memory. This is to prevent possible bus conflicts from the data bus drivers on board.

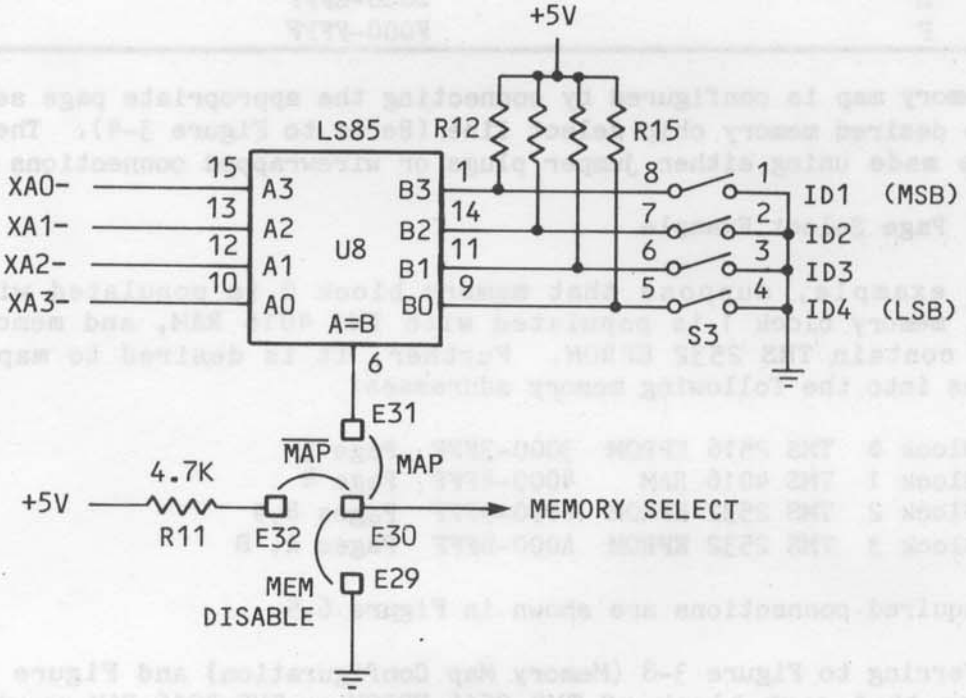


FIGURE 6-4. EXTENDED ADDRESS DECODING

6.6 MEMORY PAGE SELECTION

A page is defined as a segment of 4K contiguous bytes within a selectable address range. The allowable address ranges for the TM 990/305 are listed in Table 6-3.

TABLE 6-3. MEMORY ADDRESS BOUNDARIES

PAGE	MEMORY ADDRESSES (HEXADECIMAL)
0	0000-0FFF
1	1000-1FFF
2	2000-2FFF
3	3000-3FFF
4	4000-4FFF
5	5000-5FFF
6	6000-6FFF
7	7000-7FFF
8	8000-8FFF
9	9000-9FFF
A	A000-AFFF
B	B000-BFFF
C	C000-CFFF
D	D000-DFFF
E	E000-EFFF
F	F000-FFFF

The memory map is configured by connecting the appropriate page select line(s) to the desired memory chip select line (Refer to Figure 3-4). The connections may be made using either jumper plugs or wirewrapped connections as required.

6.6.1 Page Select Example

As an example, suppose that memory block 0 is populated with TMS 2516 EPROM, memory block 1 is populated with TMS 4016 RAM, and memory blocks 2 and 3 contain TMS 2532 EPROM. Further, it is desired to map the memory devices into the following memory addresses:

Block 0	TMS 2516 EPROM	3000-3FFF	Page 3
Block 1	TMS 4016 RAM	4000-4FFF	Page 4
Block 2	TMS 2532 EPROM	8000-9FFF	Pages 8,9
Block 3	TMS 2532 EPROM	A000-BFFF	Pages A, B

The required connections are shown in Figure 6-5.

In referring to Figure 3-8 (Memory Map Configuration) and Figure 6-5, it can be seen that each block of TMS 2516 EPROM or TMS 4016 RAM requires one page select line. When using TMS 2532 EPROM, two consecutive page select lines beginning on an even 8K-byte boundary are required to decode each block.

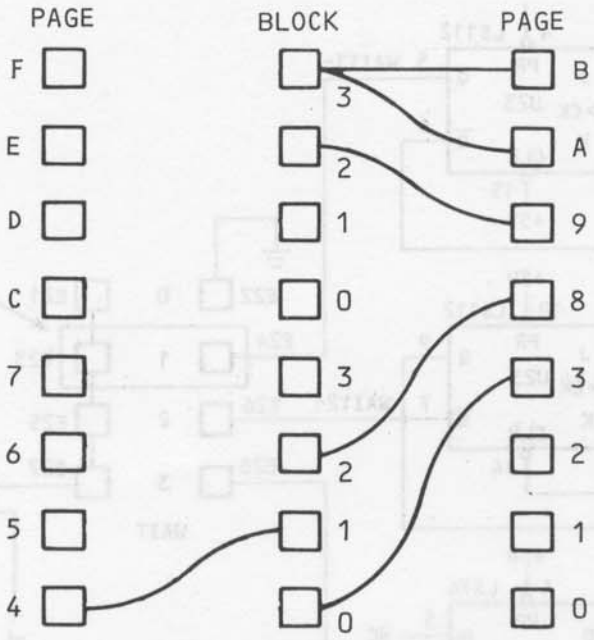


FIGURE 6-5. PAGE SELECT EXAMPLE

6.7 MEMORY ACCESS SPEED

The TMS 9900 processor interfaces easily with memories having different access times. This feature is implemented through the use of the "wait state" concept. During each memory cycle, the microprocessor samples the READY signal. When READY is active high, this indicates to the microprocessor that memory will be ready to either read or write during the next clock cycle. When READY is low during a memory operation, the TMS 9900 enters a wait state and suspends operation until the memory system indicates it is ready to proceed.

In order to select the correct number of wait states required for the slowest memory device being used, the WAIT STATE control jumper on the TM 990/305 must be positioned accordingly. Selection of up to three wait states can be implemented with this jumper. The wait state control and READY logic is shown in Figure 6-6. It can be seen that whenever no wait states are required, the READY signal is forced high.

It should be noted that the wait state jumper position controls all memory devices on the module. Therefore, if the addition or replacement of memories becomes necessary, the user must take into account the access times of the memory devices used. The slowest memory device on the module determines the number of wait states required.

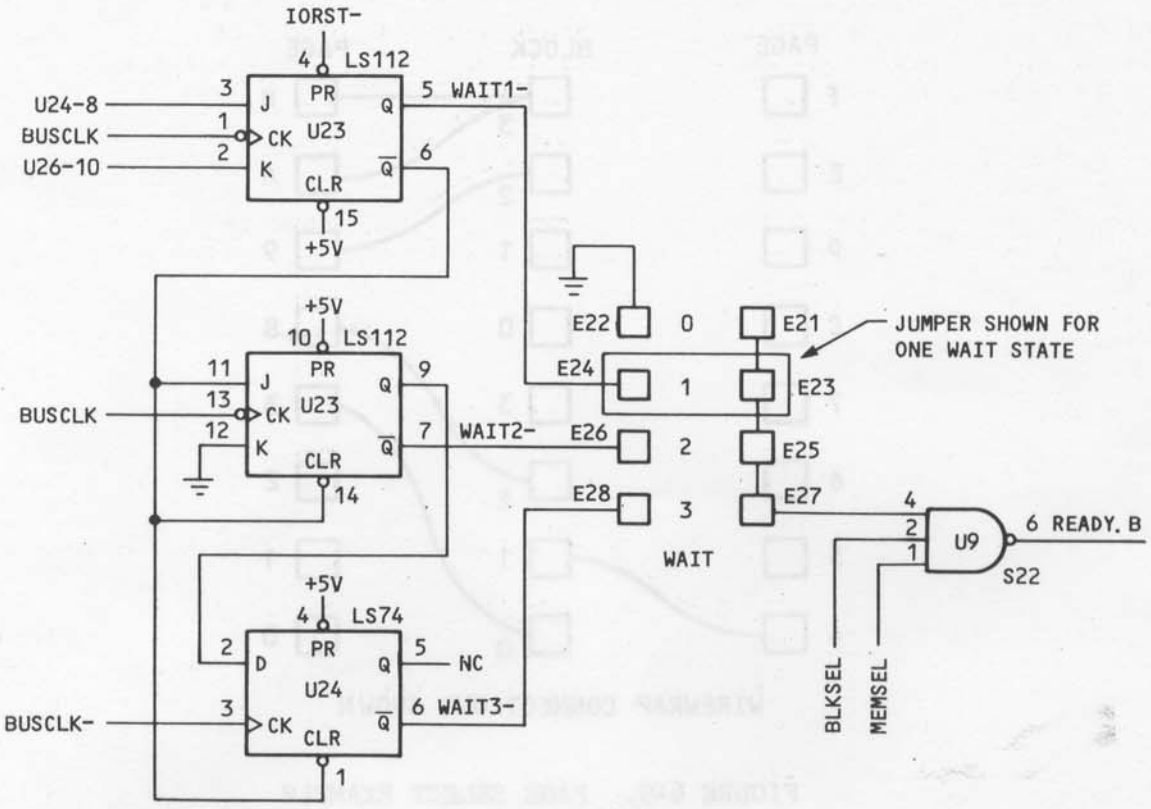


FIGURE 6-6. WAIT STATE CONTROL AND READY LOGIC

Table 6-4 contains the number of wait states required for specific memory access times with regard to the CPU system clock frequency.

TABLE 6-4. WAIT STATES

CLOCK RATE	MEMORY ACCESS TIME			
	450 ns	250 ns	200 ns	150 ns
2 MHz	0 WS	0 WS	0 WS	0 WS
3 MHz	1 WS	0 WS	0 WS	0 WS
4 MHz	1 WS	0 WS	0 WS	0 WS
5 1/3 MHz	2 WS	1 WS	0 WS	0 WS

The memory access times for the memory devices allowable on the TM 990/305 are shown in Table 6-5.

TABLE 6-5. MEMORY ACCESS TIMES

DEVICE	ACCESS TIMES
TMS 2516	450 ns
TMS 2532	450 ns
TMS 4016-15	150 ns
TMS 4016-20	200 ns
TMS 4016-25	250 ns

As an example, suppose the module were populated with TMS 2516 and TMS 2532 EPROM (each having a 450 ns access time) and the CPU used has a 3 MHz clock frequency. It can be seen from Table 6-4 that one wait state would be required. If the module were populated with TMS 4016 RAM (150, 200, or 250 ns access times) and the CPU clock frequency is also 3 MHz, no wait states would be required.

6.8 MEMORY TIMING

The memory timing for the TM 990/305 module is shown in Figure 6-7. Memory write timing is shown with no wait states and read cycle timing is shown with one.

6.9 CRU ADDRESS DECODING

For clarification in CRU addressing, the following definitions are given:

1. CRU software base address is defined as the contents of Register 12.

2. CRU hardware base address is defined as bits 3-14 of Register 12 (bit 14 is LSB).

3. CRU hardware bit address is the value as seen on address lines A3 to A14. It is generated by adding a signed displacement (from CRU instruction) to the CRU hardware base address and ensuring bits A0-A3 are all zeros.

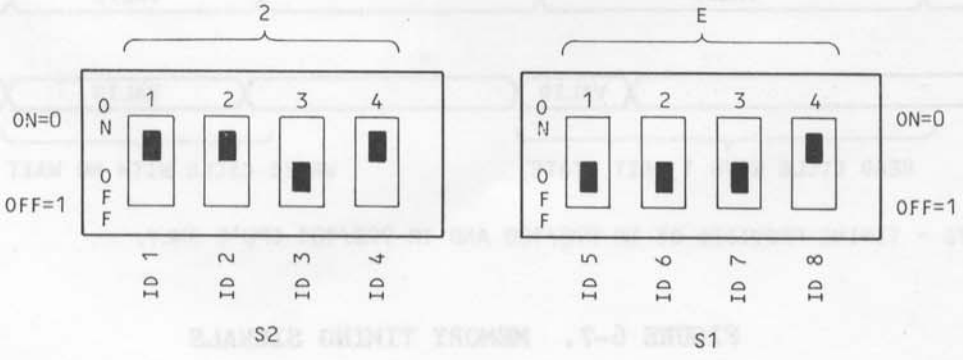
CRU base address decoding is done by comparing two 4-position DIP switches against address bits A3-A9 and ensuring the MEMEN signal is low (See Figure 6-8). Switches S2 and S1 decode hardware base addresses into blocks of 32 CRU bits. Switch S1 compares the second least significant digit in the hardware base address, while S2 compares the third least significant digit. Notice that the least significant position of S1 is electrically tied to ground, resulting in a permanent "ON" or "0" state. This forces any digit entered into S1 to be an even number.

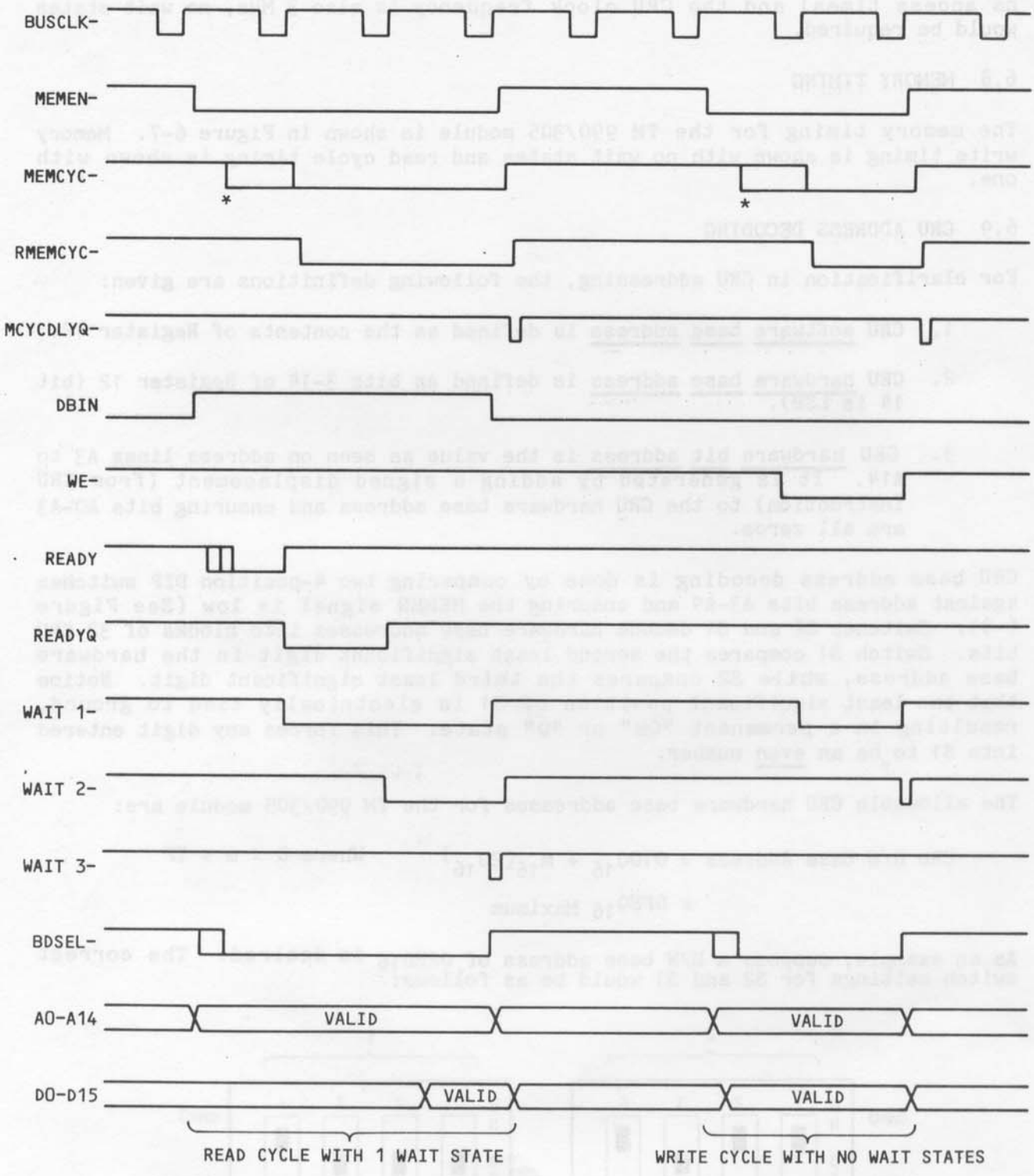
The allowable CRU hardware base addresses for the TM 990/305 module are:

$$\text{CRU H/W Base Address} = 0100_{16} + m_{16}(20_{16}) \qquad \text{Where } 0 \leq m \leq 7F$$

$$= 0FE0_{16} \text{ Maximum}$$

As an example, suppose a H/W base address of $02E0_{16}$ is desired. The correct switch settings for S2 and S1 would be as follows:





* MEMCYC - TIMING PROVIDED BY TM 990/100 AND TM 990/101 CPU'S ONLY.

FIGURE 6-7. MEMORY TIMING SIGNALS

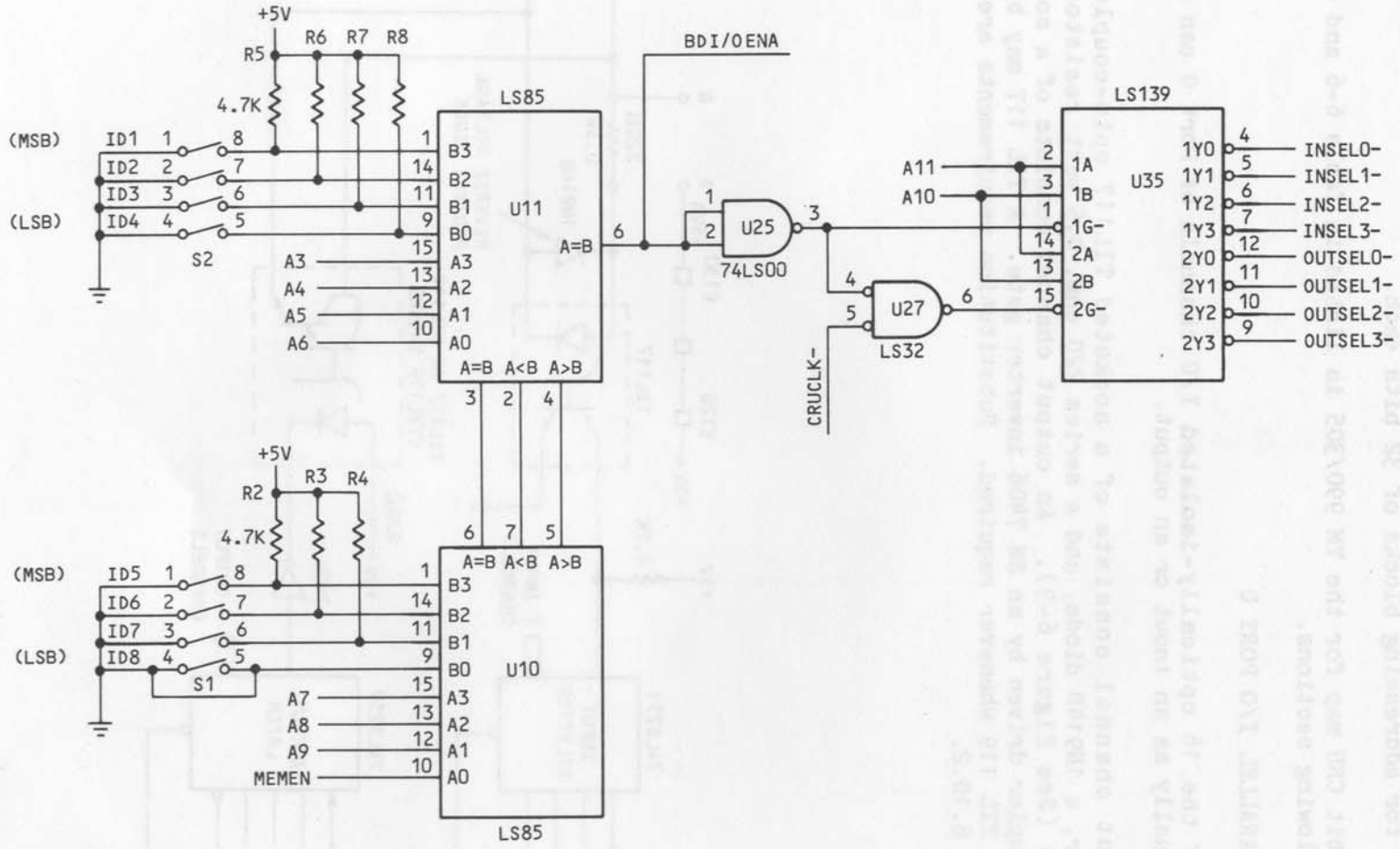


FIGURE 6-8. CRU HARDWARE BASE ADDRESS DECODE

Whenever the CRU address presented on the bus agrees with the switch settings, an enable signal (BDI/OENA) is generated. This signal, along with CRUCLK-, is gated to a 74LS139 decoder, where address bits A10 and A11 are combined to generate the appropriate I/O select lines. Each select line enables 8 CRU bits as inputs (e.g. INSEL0-) or as outputs (e.g. OUTSEL0-). Since address bits A3-A9 are used to decode the hardware base address, this leaves bits A10-A14 for addressing blocks of 32 bits each.

The 32-bit CRU map for the TM 990/305 is listed in Table 6-6 and explained in the following sections.

6.10 PARALLEL I/O PORT 0

Each of the 16 optically-isolated I/O channels of Port 0 can be configured individually as an input or an output.

An input channel consists of a socketed TIL117 opto-coupler, a pullup resistor, a 1N914B diode, and a series 220 ohm, 0.5 watt resistor mounted in sockets (See Figure 6-9). An output channel consists of a socketed TIL119 opto-coupler driven by an SN 7406 inverter gate. A TIL 117 may be substituted for the TIL 119 whenever required. Substitution requirements are explained in Section 6.10.2.

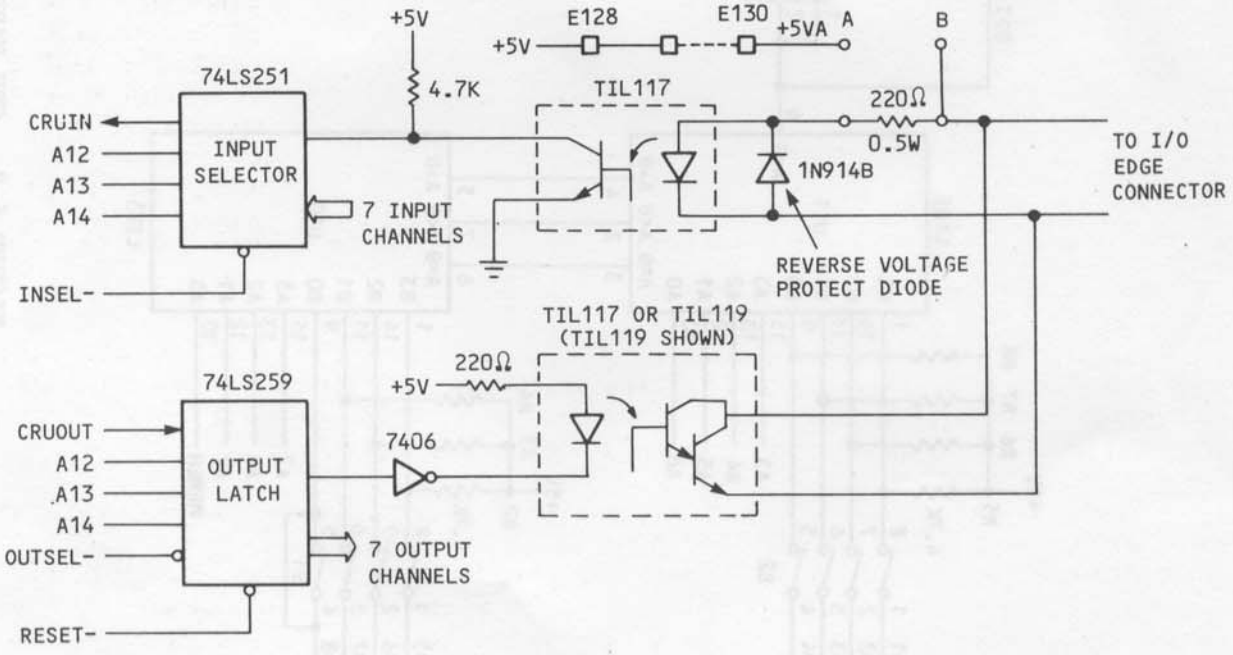


FIGURE 6-9. I/O CHANNEL

TABLE 6-6. CRU MAP

Definitions: A = CRU H/W Base Address (R12, Bits 3-14)
S/W Base Address = 2 X H/W Bit Address

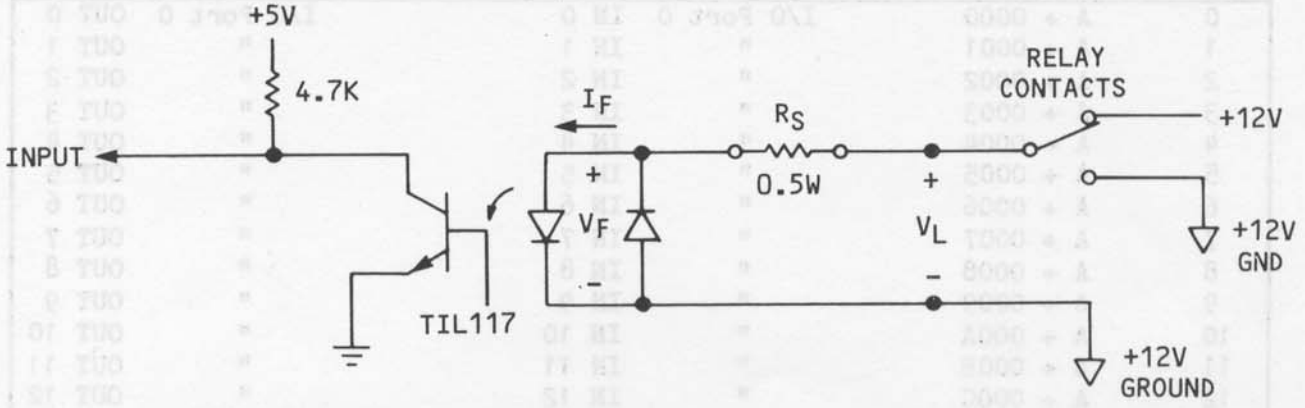
CRU Bit	H/W Bit Address	Input	Output
0	A + 0000	I/O Port 0 IN 0	I/O Port 0 OUT 0
1	A + 0001	" IN 1	" OUT 1
2	A + 0002	" IN 2	" OUT 2
3	A + 0003	" IN 3	" OUT 3
4	A + 0004	" IN 4	" OUT 4
5	A + 0005	" IN 5	" OUT 5
6	A + 0006	" IN 6	" OUT 6
7	A + 0007	" IN 7	" OUT 7
8	A + 0008	" IN 8	" OUT 8
9	A + 0009	" IN 9	" OUT 9
10	A + 000A	" IN 10	" OUT 10
11	A + 000B	" IN 11	" OUT 11
12	A + 000C	" IN 12	" OUT 12
13	A + 000D	" IN 13	" OUT 13
14	A + 000E	" IN 14	" OUT 14
15	A + 000F	" IN 15	" OUT 15
16	A + 0010	INPUT PORT1 IN0/INTERRUPT 0	INTERRUPT RESET 0
17	A + 0011	" IN1/INTERRUPT 1	INTERRUPT RESET 1
18	A + 0012	" IN2/INTERRUPT 2	INTERRUPT RESET 2
19	A + 0013	" IN3/INTERRUPT 3	INTERRUPT RESET 3
20	A + 0014	" IN4	
21	A + 0015	" IN5	
22	A + 0016	" IN6	
23	A + 0017	" IN7	
24	A + 0018	" IN8	INTERRUPT MASK 0
25	A + 0019	" IN9	INTERRUPT MASK 1
26	A + 001A	" IN10	INTERRUPT MASK 2
27	A + 001B	" IN11	INTERRUPT MASK 3
28	A + 001C	" IN12	STATUS LED #1
29	A + 001D	" IN13	STATUS LED #2
30	A + 001E	" IN14	BOARD I/O RESET
31	A + 001F	" IN15/BOARD INTERRUPT	BOARD INTER. RESET

6.10.1 Input Channel Configuration

To configure a channel as an input, it is recommended that the output opto-coupler be removed from its socket. If not removed, then the SN7406 inverter driving it must be programmed to ensure the opto-coupler is not conducting, i.e., the output of the SN7406 must be high.

An input signal of sufficient magnitude is required to ensure a forward voltage drop of 1.2 V across the input diode of the TIL117. The purpose of the series resistor is to limit the current through the input diode to approximately 15 mA. Knowing this voltage and current requirement, the user may replace the series resistor with a resistor of different value depending on the voltage being input to the channel.

As an example, suppose the requirement is to monitor a 12 V relay for contact closure. This could be implemented in the following manner:



R_S would be selected using the equation:

$$R_S = (V_L - V_F)/ I_F$$

Where V_L = Line Voltage

V_F = Forward Voltage Drop

I_F = Input Current

$$= (12-1.2)/(0.015)$$

$$= 720 \text{ ohms}$$

CAUTION

The user must not exceed the electrical ratings of the input/output circuitry as set forth in Appendix A.

Each input channel is connected to a 74LS251 data selector which when selected presents the input signal to the processor via the CRUIN line. Address bits A12-A14 select which of the 8 input channels is to be transmitted as CRU input data. As an example, suppose that an input signal of proper magnitude were present at the edge connector. The input diode of the TIL117 would conduct, causing the output phototransistor to saturate to approximately 0.4 volts. This would be recognized by the input selector and output on the CRUIN line as a logic "0".

6.10.2 Output Channel Configuration

To configure a channel as an output, the user may remove the input series resistor, R_S, from its socket. Either a TIL117 or TIL119 opto-coupler may be used depending on the output voltage/current requirements. The TIL117 has an output phototransistor which is compatible with TTL logic gates. The TIL119 has an output photodarlington transistor designed for higher current-carrying capability.

Each output channel receives its output signal from a 74LS259 latch. When properly addressed and selected, the output latch configures the I/O channel according to the data presented on the CRUOUT line. As an example, suppose that a logic "1" is presented to the addressed output latch via the CRUOUT line. This drives the output of the 7406 low, causing the input diode of the output optical isolator to conduct. This drives the output transistor to a saturated state. If the input series resistor R is not removed, then the state of the output can be read. In this case, an output ON state is read as a ZERO, and an OFF state is read as a ONE. This mode can be called echo-back output.

6.10.3 Polarity Inversion

It is important for the user to understand that polarity inversion occurs whenever using optical couplers in this configuration. An input logic "1" at the edge connector is seen by the processor as a logic "0". Similarly, an output logic "1" is seen at the edge connector as a logic "0".

The 7406 inverting drivers in the output circuits may be replaced with 7407 non-inverting drivers if output polarity inversion is not desired. Note, however, that when using echo-back output, the logical value read is always the inverse of the logical value of the output, no matter how the output is driven.

NOTE

If the 7406 in the U44 position is changed to a 7407, polarity inversion will occur in output bits 12-15 and also the control polarity of the two STATUS LEDs (DS1 and DS2) will be reversed.

6.10.4 Port 0 Reset

There are 3 ways to reset the 74LS259 output latches on Port 0:

1. The CRU instruction SBZ resets individual channels, while the instruction LDCR can reset the entire port if specified in the instruction. Refer to Section 5 for programming information.

2. Writing a bit, either a ONE or a ZERO, to the CRU bit designated BOARD I/O RESET.

3. The processor-generated signal, IORST. See Section 6.11.5 for an explanation of this signal.

6.10.5 5MT Interface

Shown in Figure 6-9 are sockets A and B and a jumper connection to +5 V. When interfacing the TM 990/305 to a 5MT industrial I/O system, the user must insert a 680 ohm, 0.5 watt pullup resistor (R85-R100) between sockets A and B for each configured channel and connect these to +5 V by a single jumper plug (E129 to E130). A TM 990/509 cable would then be used to connect the TM 990/305 to the 5MT. The appropriate connections are explained in Appendix F.

When configuring a channel as an output, a TIL 117 optical isolator must be placed in the output position of the socket, and the 220Ω 0.5 W series input resistor must be removed. When configuring a channel as an input, the output

opto-isolator must be removed from its socket.

NOTE

> The reset signal IORST (from the logical OR of power-up reset, the RESET switch on the microcomputer board, or the RSET external instruction) will force all configured output channels of Port 0 to the high state; therefore, all 5MT outputs will be initially active. The user who finds this feature undesirable may replace the SN7406 inverting drivers (positions U44, U47, U48 and U51) with SN7407 non-inverting drivers. Execution of the IORST-signal would then cause all 5MT outputs to be initially inactive.

To turn on an output module, the controlling program must write a "ZERO" to the addressed output module through the CRU. Writing a "ONE" to an output module turns off the load.

When reading an input module, a "ONE" will be read through the CRU whenever the rated input signal voltage is applied to the module's input. Likewise, when the input module senses no voltage, the program will read a "ZERO".

It is IMPORTANT that the programmer understands this convention in order to properly control the 5MT system.

6.11 PARALLEL INPUT PORT 1

Port 1 consists of 16 optically-isolated input channels. Channels 0-3 may be configured individually either as standard inputs or edge-triggered interrupt inputs. When configured as interrupts, channels 0 and 2 are negative edge-triggered, while channels 1 and 3 are positive edge-triggered. Channels 4-14 are dedicated as standard inputs. Channel 15 may be configured either as a standard input channel or edge-triggered board interrupt input. Figure 6-10 is a diagram of channels 0-3 and 15 and Figure 6-11 is a diagram of standard input channels 4-14.

When channels 0-15 are configured as standard inputs, their operation is identical to the input channels of Port 0.

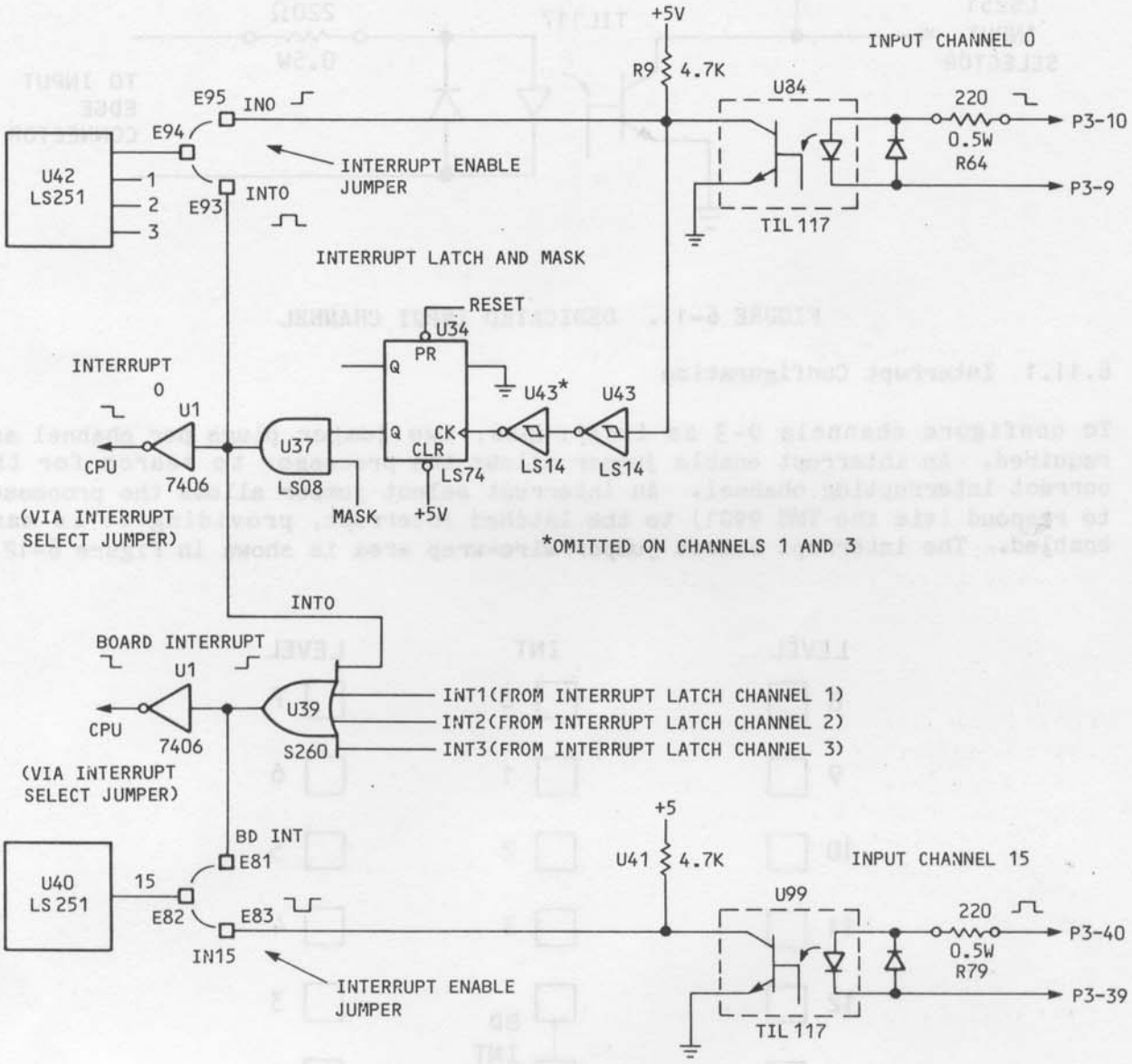


FIGURE 6-10. CONFIGURABLE INPUT CHANNELS

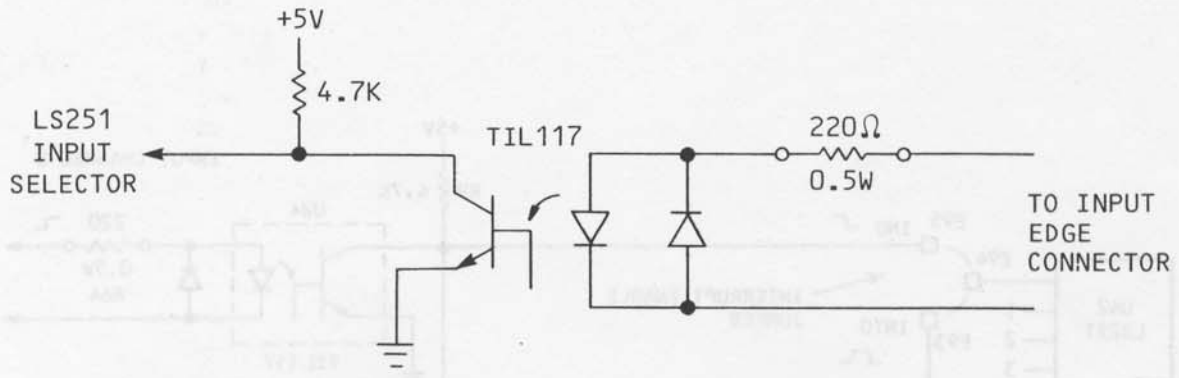


FIGURE 6-11. DEDICATED INPUT CHANNEL

6.11.1 Interrupt Configuration

To configure channels 0-3 as interrupts, two jumper plugs per channel are required. An interrupt enable jumper allows the processor to search for the correct interrupting channel. An interrupt select jumper allows the processor to respond (via the TMS 9901) to the latched interrupt, providing it is mask enabled. The interrupt select jumper/wire-wrap area is shown in Figure 6-12.

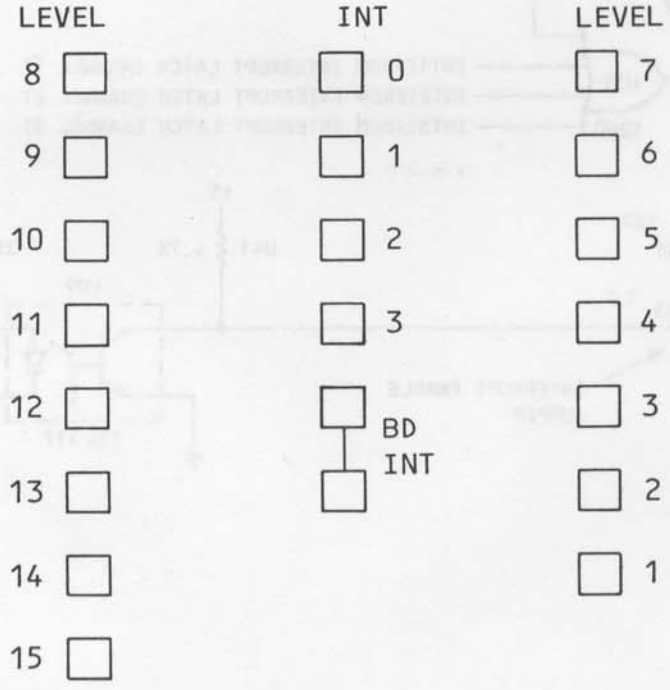


FIGURE 6-12. INTERRUPT SELECT

Interrupt sources 0-3 and board interrupt may be connected to CPU interrupt levels 1-15 in any desired configuration.

To configure channel 15 as a board interrupt, its appropriate interrupt select and interrupt enable jumpers must be positioned correctly. A board interrupt signal is generated by "OR-ing" together masked interrupts 0-3. In other words, whenever any masked interrupt occurs on the module, a board interrupt signal is generated. If several TM 990/305 modules are used in a system, the board interrupt signal allows the CPU to search for the interrupting module before interrogating the individual interrupts on that module.

6.11.2 Interrupt Mask

Each of the four interrupts 0-3 must be enabled by an appropriate CRU addressable MASK bit. By writing a "1" to the MASK bit, that interrupt then becomes enabled. The interrupt is disabled by writing a "0" to its MASK bit.

6.11.3 Interrupt Reset

INTRST0- through INTRST3- individually reset interrupts 0-3 respectively. These are generated from a 74LS139 decoder upon writing a bit, either a ONE or a ZERO, to the CRU bits designated RES0 through RES3 corresponding to interrupts 0-3 respectively. The signals BDINTRST- and BDI/ORST- also may be used to reset the interrupts and are explained in the following sections.

6.11.4 Board Interrupt Reset

Writing a bit, either a ONE or a ZERO, to the CRU bit designated BOARD INTERRUPT RESET accomplishes the following:

1. Drives the latches for interrupts 0-3 to an unlatched state
2. Resets Interrupt Masks 0-3, disabling the four interrupts
3. Turns both status LEDs off.

6.12 BOARD I/O RESET

Writing a bit, either a ONE or a ZERO, to the CRU bit designated BOARD I/O RESET performs the same function as BOARD INTERRUPT RESET in Section 6.11.3. In addition, it resets the 74LS259 output latches for Port 0.

6.13 I/O RESET

A processor-generated signal called IORST is caused by either: 1) actuating the RESET switch on the CPU module, 2) setting the PRES.B signal to a logic ZERO state on connector P1 (Pin 94), or 3) executing an RSET instruction. The IORST signal performs the same function on the TM 990/305 as BOARD I/O RESET in Section 6.12.

6.14 STATUS INDICATORS

A status indicator is a CRU-addressable light-emitting diode (LED). Two indicators, designated DS1 and DS2, are located on the TM 990/305 module between connectors P2 and P3. Writing a ONE to the appropriate CRU address turns the LED on; writing a ZERO turns the LED off.

These indicators may be used by the programmer to display a particular status. Initialization software can turn the LEDs off after initialization is complete. Stages 0-3 of a particular operation may be displayed by turning the appropriate LEDs on. A system error can cause an LED to come on. Test software can cycle the LEDs during execution. Uses for these LEDs are

limited only by the imagination.

Upon power-up, both LEDs are turned off unless 7407 drivers are used in the U44 position (See Section 6.10.3).

6.15 ADDRESS AND CONTROL BUFFERS

The address and control buffers consist of four octal line drivers/receivers in positions U4-U7 and a bus buffer gate in position U38. Address bits A0-A14 are brought on board the module, along with extended address bits XA0-XA3.

Buffered control signals include the memory read/write signals, CRU lines, IORST-, and the system clock BUSCLK.

6.16 DATA BUFFERS

Two LS245 octal bus transceivers (positions U2 and U3) accommodate data bus transfer. Direction of the data flow is controlled by the signal DBIN during a memory operation.

APPENDIX A

INPUT/OUTPUT ELECTRICAL RATINGS

A.1 GENERAL

All specifications apply over the full temperature range of 0-70°C, except as noted. All currents and voltages are DC.

A.2 INPUT ELECTRICAL RATINGS

Input Circuit (R_S = 220Ω)	MIN	TYP	MAX	UNIT
ON Voltage	3.8			V
Continuous ON Voltage			8.5	V
Continuous ON Current	12		34	mA
Reverse Polarity			30	V
Continuous Reverse polarity			18	V
Input to Output Isolation Voltage			500	V
Input to Output Resistance	10^{11}			Ω
Input Circuit (CUSTOMER SUPPLIED R_S)				
ON Voltage	3.3			V
Continuous ON Voltage			30	V
Continuous ON Current	12		34	mA
Power Dissipation in R_S			0.25	W
Reverse Polarity			30	V
Input to Output Isolation Voltage			500	V
Input to Output Resistance	10^{11}			Ω

A.3 OUTPUT ELECTRICAL RATINGS

Output Circuit (TTL OPTION-TIL117)	TEST COND	MIN	TYP	MAX	UNIT
OFF State Collector Current	VCE=10V			50	nA
Collector-Emitter Saturation Voltage	Ic=2mA			0.4	V
Collector-Emitter Breakdown Voltage				30	V
Emitter-Collector Breakdown Voltage				7	V
Power Dissipation Per Output @ 25°C*				150	mW
Input to Output Isolation Voltage				500	V
Input to Output Resistance		10^{11}			Ω
Output Circuit (CURRENT OPTION-TIL119)					
OFF State Collector Current	VCE=10V			100	nA
Collector-Emitter Saturation Voltage	Ic=30mA			1	V
Collector-Emitter Breakdown Voltage				30	V
Emitter-Collector Breakdown Voltage				7	V
Power Dissipation Per Output @ 25°C*				150	mW
Input to Output Isolation Voltage				500	V
Input to Output Resistance		10^{11}			Ω

* Derate linearly to 70°C at 2mW/°C.

APPENDIX B

PARTS LIST

TABLE B-1. PARTS FOR TM 990/305 MODULE

Symbol	Description
C1, C38, C39	Capacitor, 22 uF @ 15 V
C2	Capacitor, 68 uF @ 15 V
C3-C37	Capacitor, .1 uF @ 50 V
CR1-CR33	Diode, 1N914B
DS1, DS2	Optoelectronic Device, TIL220
R1-R16, R19, R20, R23, R24 R27, R28, R31, R32, R35, R36, R39, R40, R43, R44, R47	Resistor, 4.7K Ohm 5% .25W
R17, R18, R21, R22, R25, R26, R29, R30, R33, R34, R37, R38, R41, R42, R45, R46	Resistor, 220 Ohm 5% .25W
R48-R79 (See Note 1)	Resistor, 220 Ohm 5% .5W
R80-R84, R101	Resistor, 330 Ohm 5% .25W
S1, S2, S3	Switch Dual In Line, 4 Position
VR1	IC, Pos Voltage Regulator, 3-Pin, TO-220AB, UA7808C
U1, U44, U47, U48, U51	Network, SN7406N
U2, U3	Network, SN74LS245N
U4, U7	Network, SN74LS241N
U5	Network, SN74S241N
U6	Network, SN74S240N
U8, U10, U11	Network, SN74LS85N
U9	Network, SN74S22N
U20, U28	Network, 74LS145N
U21	Network, SN74S20N
U22, U24, U30, U34	Network, SN74LS74N
U23	Network, SN74LS112N
U25	Network, SN74LS00N
U26	Network, SN74LS02N
U27	Network, SN74LS32N
U29	Network, SN74S32N
U31, U36, U37	Network, SN74LS08N
U32, U35	Network, SN74LS139N
U33, U46, U50	Network, SN74LS259N
U38	Network, SN74LS126N
U39	Network, SN74S260N
U40, U42, U45, U49	Network, SN74LS251N
U41	Resistor, Fixed-Array, 4.7K
U43	Network, SN74LS14N
U52-U55 (See Note 2)	IC, Optically Coupled Isolator, TIL119
U68-U83	IC, Optically Coupled Isolator, TIL117

TABLE B-1. PARTS FOR TM 990/305 (CONCLUDED)

Symbol	Description
XU12-XU19	Socket, 24 Pin IC Low Profile Solder Tail
XU52-XU99, XU44, XU47, XU48, XU51	Socket, 14 Pin IC Low Profile Solder Tail

NOTES

1. Socketed resistors R48-R79 and R85-R100 (user-supplied) are required to have .031 ± .002 lead diameters. Some appropriate vendors and types are:

   R-OHM Corp. Type R-50 carbon film
   16931 Milliken Ave.
   P. O. Box 19515
   Irvine, Calif. 92713
   (714) 546-7750 or (312) 843-0404

   ADI Electronics Inc. Type ADI-50 carbon film
   160 Wilbur P1.
   Bohemia, N. Y. 11716
   (516) 567-3555

2. U52-U67 will accept TIL117 or TIL119.

APPENDIX C

SCHEMATICS

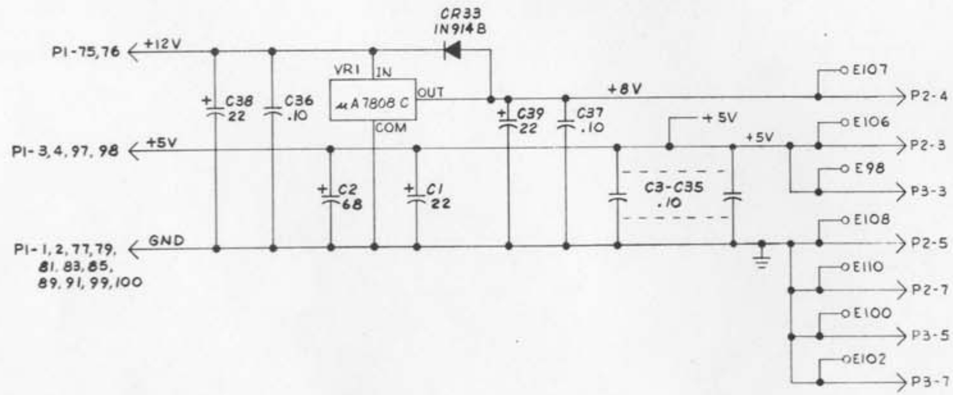
NOTES: UNLESS OTHERWISE SPECIFIED:

1. ALL CAPACITOR VALUES ARE IN MICROFARADS
2. RESISTOR VALUES ARE IN OHMS
3. ALL RESISTORS TO BE .25 W, 5 %
4. SOCKETS AT POSITIONS U12-U19 WILL ACCEPT DEVICE TYPES TMS 4016, TMS 2516, OR TMS 2532, USER'S OPTION
5. 7407 NON-INVERTING DRIVERS (OPEN COLL.) MAY BE SUBSTITUTED FOR THESE SOCKETED DEVICES BY THE USER
6. DEVICES SHOWN FOR CLARITY. ACTUAL COMPONENTS INSTALLED BY USER
7. SOCKETS WILL ACCEPT EITHER TIL117 OR TIL119 OPTICAL ISOLATORS
8. RESISTORS R48-R79 INSTALLED IN SOCKETS
9. ALL 0.5 W RESISTORS INSTALLED IN SOCKETS REQUIRE .031±.002 LEAD DIAMETERS

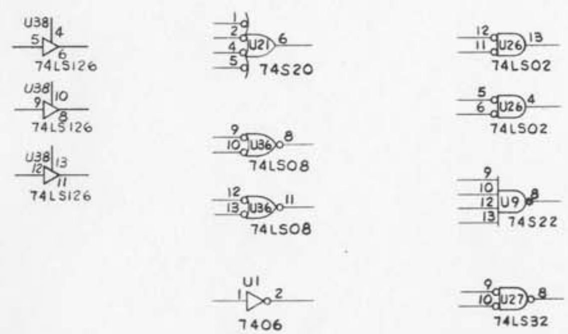
DEVICE TYPE	REFERENCE DESIGNATORS	PIN NOS. +5 V	PIN NOS. GND
74LS00	U25	14	7
74LS02	U26	14	7
7406	U1, U44, U47, U48, U51	14	7
74LS08	U31, U36, U37	14	7
74LS14	U43	14	7
74S20	U21	14	7
74S22	U9	14	7
74S32	U29	14	7
74LS32	U27	14	7
74LS74	U22, U24, U30, U34	14	7
74LS85	U8, U10, U11	16	8
74LS112	U23	16	8
74LS126	U38	14	7
74LS139	U32, U35	16	8
74LS145	U20, U28	16	8
74S240	U6	20	10
74S241	U5	20	10
74LS245	U2, U3	20	10
74LS251	U40, U42, U45, U49	16	8
74LS259	U33, U46, U50	16	8
74S260	U39	14	7
74LS241	U4, U7	20	10

REFERENCE DESIGNATORS USED	NOT USED
C1-C39	
CR1-CR33	
DS1, DS2	
E1-E134	
P1-P3	
R1-R101	
S1-S3	
U1-U99	
VR1	

JUMPER CONFIGURATIONS		
E8, E16	E40, E41	E64, E76
E9, E17	E43, E44	E82, E83
E10, E18	E46, E47	E85, E86
E11, E19	E49, E50	E88, E89
E12, E20	E52, E53	E91, E92
E21, E22	E55, E56	E94, E95
E30, E32	E61, E73	E128, E129
E34, E35	E62, E74	E131, E132
E37, E38	E63, E75	



SPARES



QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION	NOTES

PARTS LIST

NEXT ASSY	USED ON
1600046	8117
1600045	8117

APPLICATION

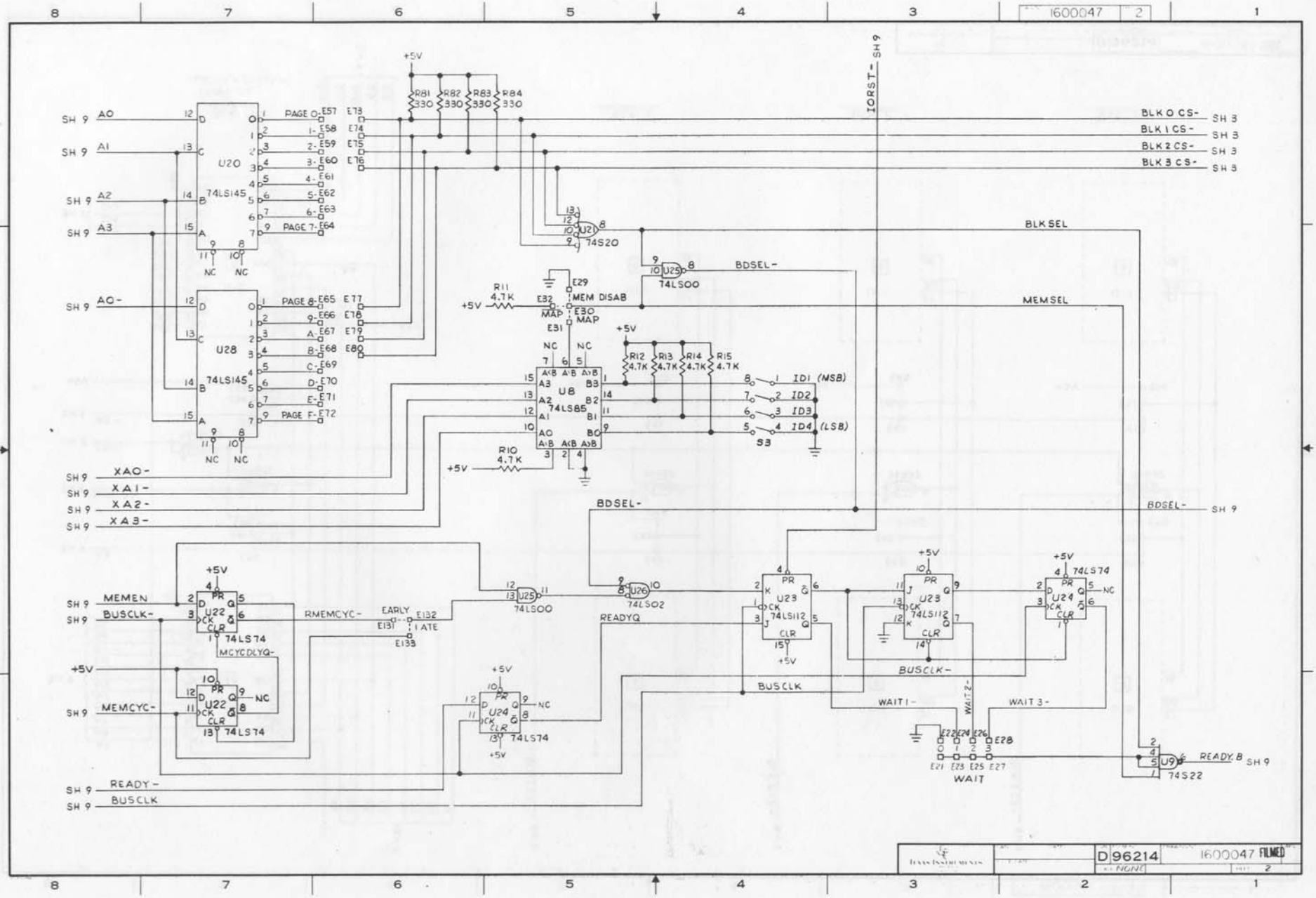
TEXAS INSTRUMENTS INCORPORATED Dallas, Texas

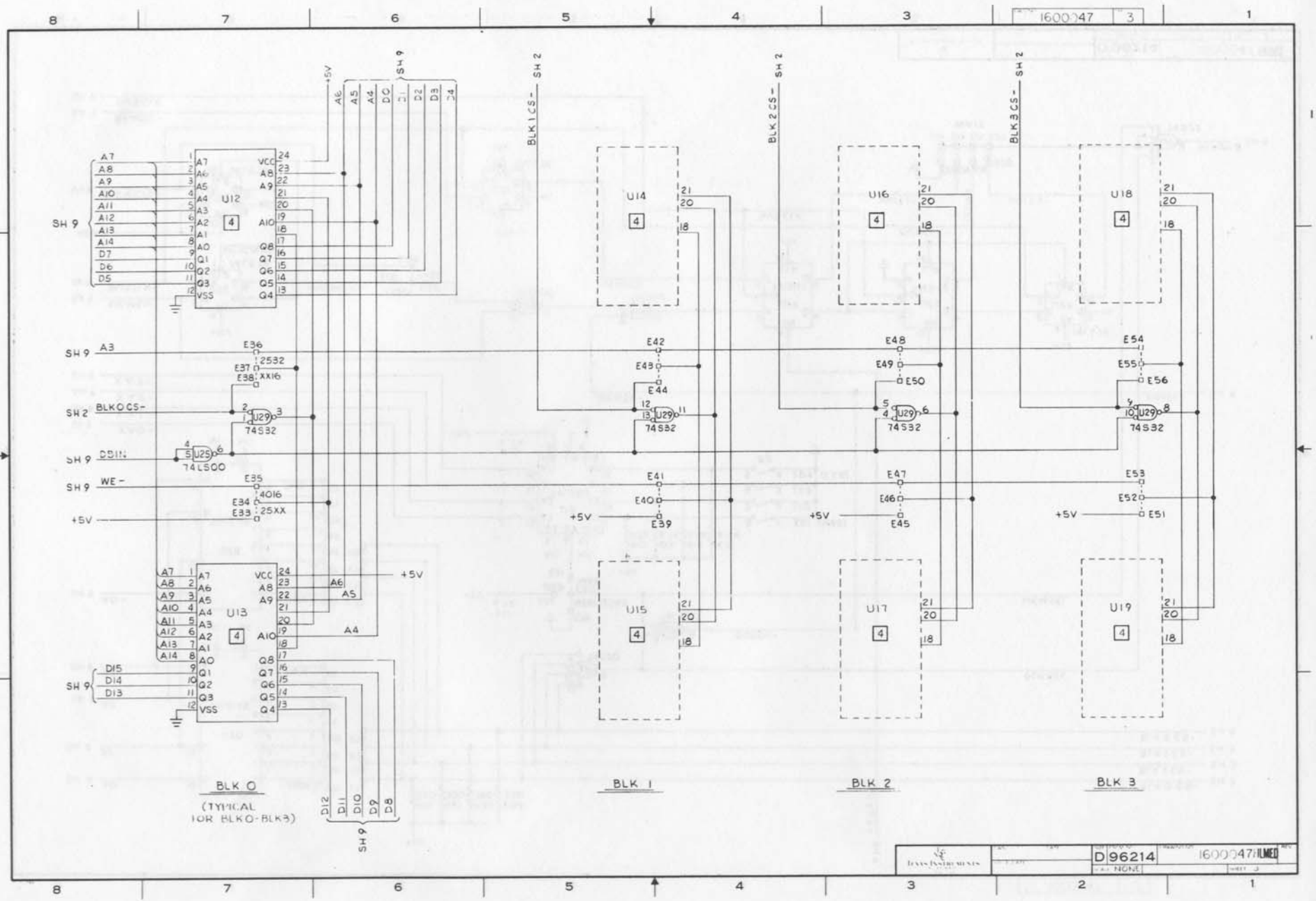
DIAGRAM, LOGIC
TM 990/305

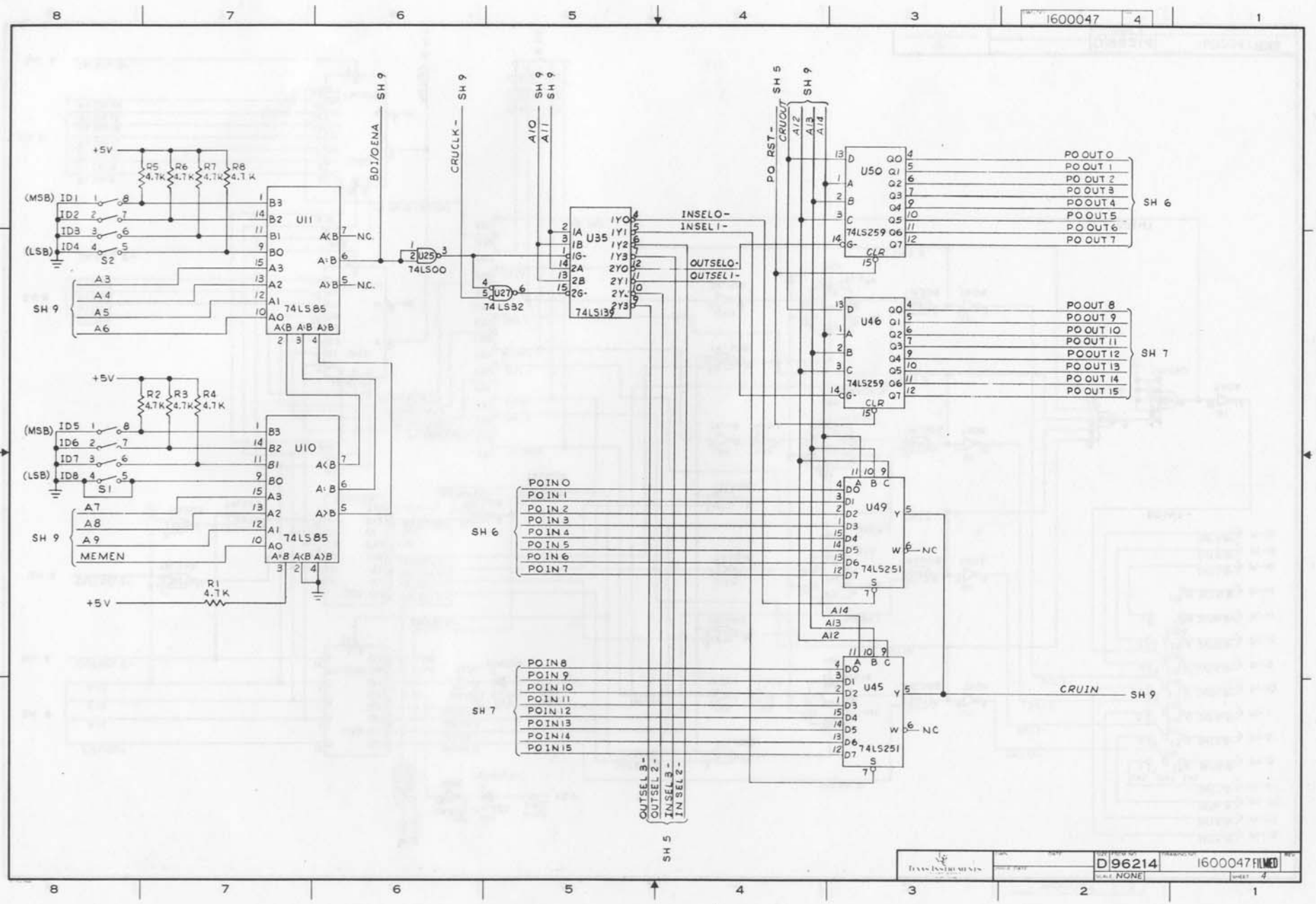
D 96214 1600047 FILMED
SCALE NONE SHEET 1 OF 9

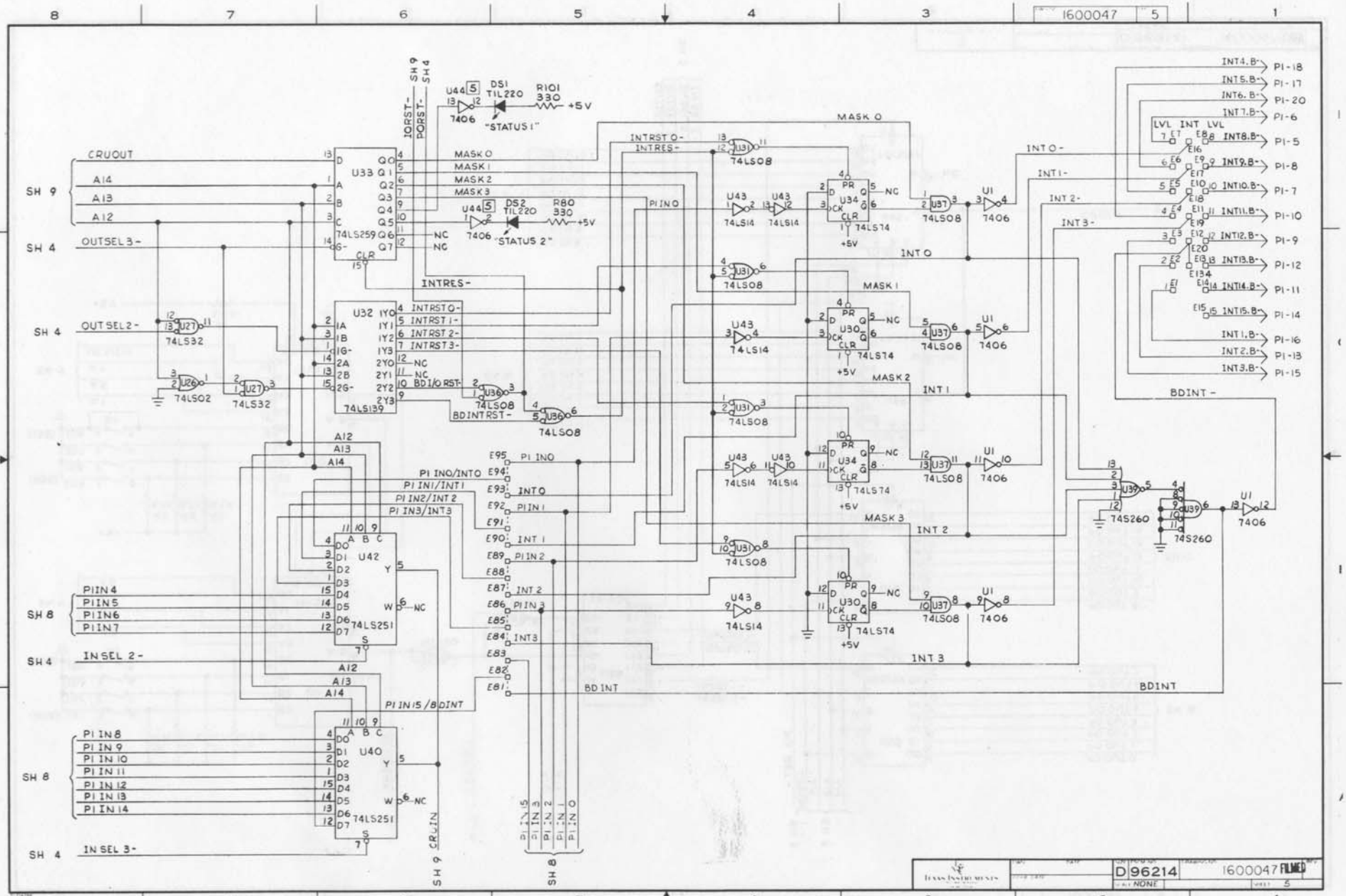
REVISIONS
DWG NO 1600047 SH 1

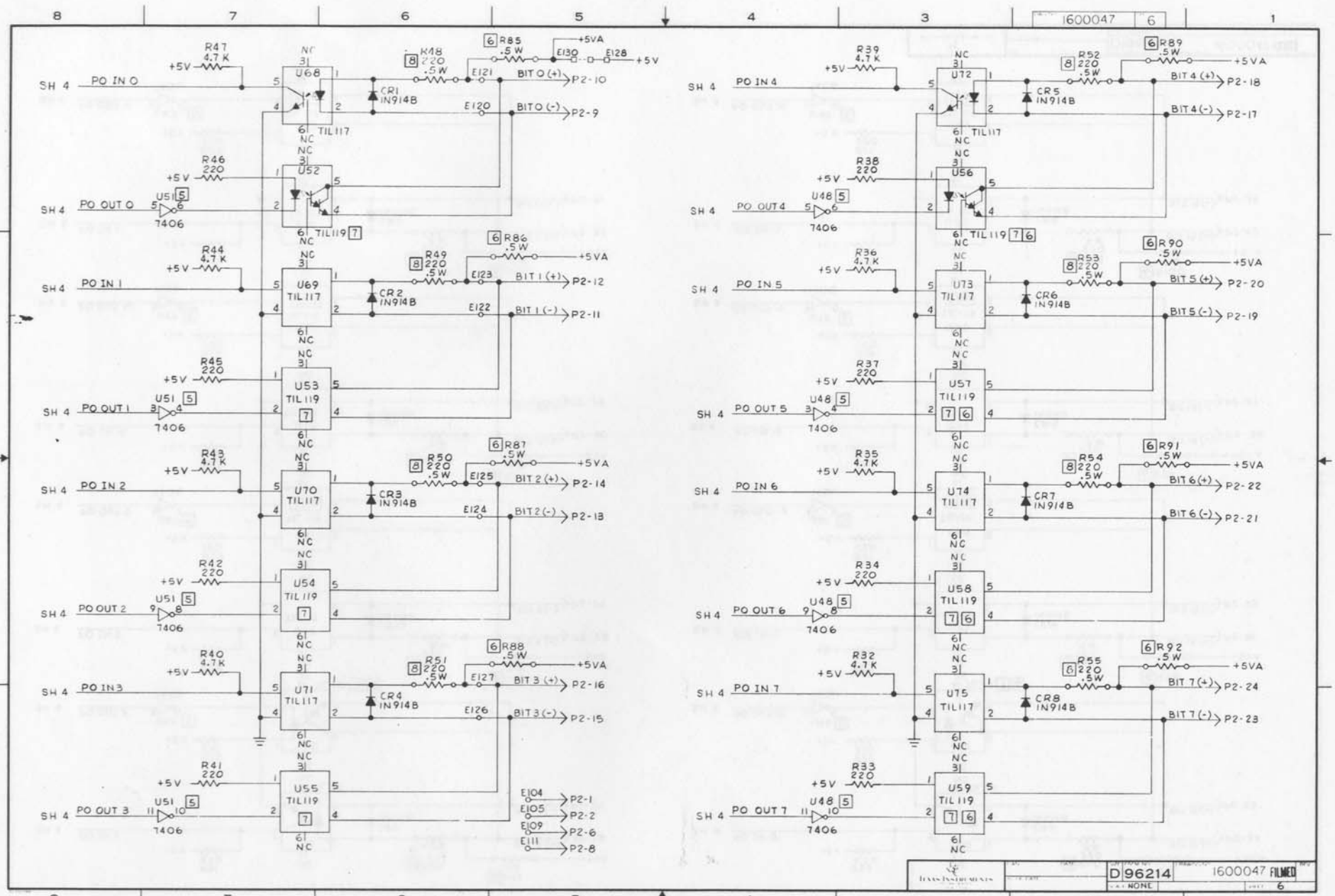
SEQ NO | IDENT | F SPEC | NO | ADDITIONAL | NOTES
PROCESS | CLASSIFICATION
PROCESSES — FOR CORRELATION TO GOVT/IND SPECIFICATIONS SEE TI DRAWING 729487

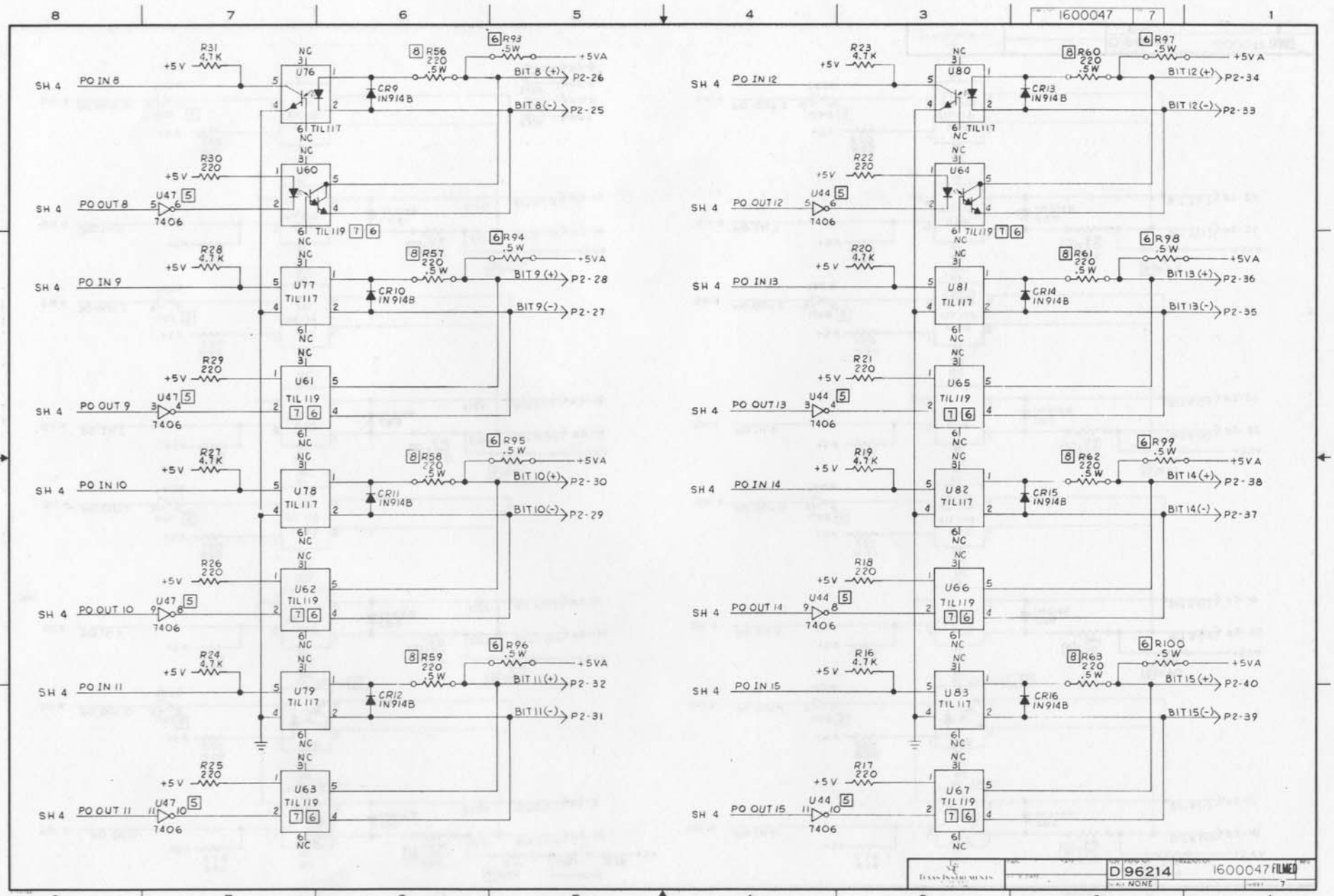

1600047 2
U20
74LS145
U28
74LS145
U8
74LS85
U21
74S20
U25
74LS00
U26
74LS02
U23
74LS112
U24
74LS74
U22
74LS74
U9
74S22
R81 330
R82 330
R83 330
R84 330
R11 4.7K
R10 4.7K
R12 4.7K
R13 4.7K
R14 4.7K
R15 4.7K
+5V
IORST- SH 9
BLK0 CS- SH 3
BLK1 CS- SH 3
BLK2 CS- SH 3
BLK3 CS- SH 3
BLKSEL
BDSEL-
MEMSEL
MEM DISAB
MAP
ID1 (MSB)
ID2
ID3
ID4 (LSB)
S3
XA0-
XA1-
XA2-
XA3-
MEMEN
BUSCLK-
RMEMCYC-
EARLY
LATE
MCYCDLYQ-
MEMCYC-
READYQ
BUSCLK
WAIT1-
WAIT2-
WAIT3-
WAIT
READY-
READY.B
D 96214
1600047 FILMED


1600247 3
SH 9
SH 2
BLK1CS-
BLK2CS-
BLK3CS-
U12
U13
U14
U15
U16
U17
U18
U19
74S32
74LS00
2532
XX16
4016
25XX
BLK 0
(TYPICAL
FOR BLK0-BLK3)
BLK 1
BLK 2
BLK 3
D96214
1600247
NONE

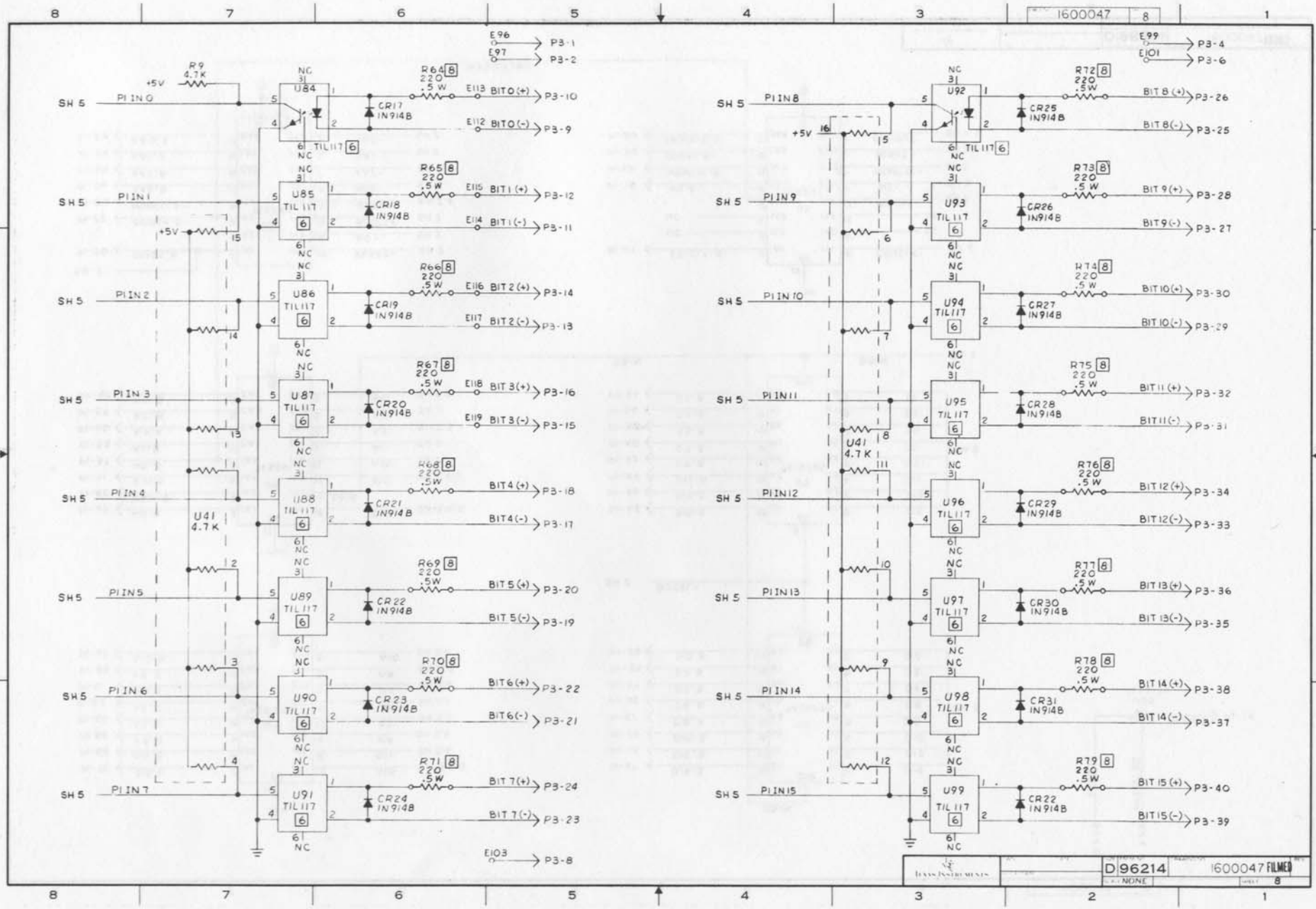

1600047 4
U11
U10
U35
U50
U46
U49
U45
74LS85
74LS00
74LS32
74LS139
74LS259
74LS251
+5V
R1 4.7K
R2 4.7K
R3 4.7K
R4 4.7K
R5 4.7K
R6 4.7K
R7 4.7K
R8 4.7K
(MSB) ID1
ID2
ID3
(LSB) ID4
S2
(MSB) ID5
ID6
ID7
(LSB) ID8
S1
MEMEN
BDI/OENA
CRUCLK-
A10
A11
PO RST-
CRUOUT
A12
A13
A14
INSELO-
INSEL1-
OUTSELO-
OUTSEL1-
PO OUT 0
PO OUT 1
PO OUT 2
PO OUT 3
PO OUT 4
PO OUT 5
PO OUT 6
PO OUT 7
PO OUT 8
PO OUT 9
PO OUT 10
PO OUT 11
PO OUT 12
PO OUT 13
PO OUT 14
PO OUT 15
PO IN 0
PO IN 1
PO IN 2
PO IN 3
PO IN 4
PO IN 5
PO IN 6
PO IN 7
PO IN 8
PO IN 9
PO IN 10
PO IN 11
PO IN 12
PO IN 13
PO IN 14
PO IN 15
CRUIN
OUTSEL 3-
OUTSEL 2-
INSEL 3-
INSEL 2-
SH 5
SH 6
SH 7
SH 9
NC
D 96214
1600047 FILMED

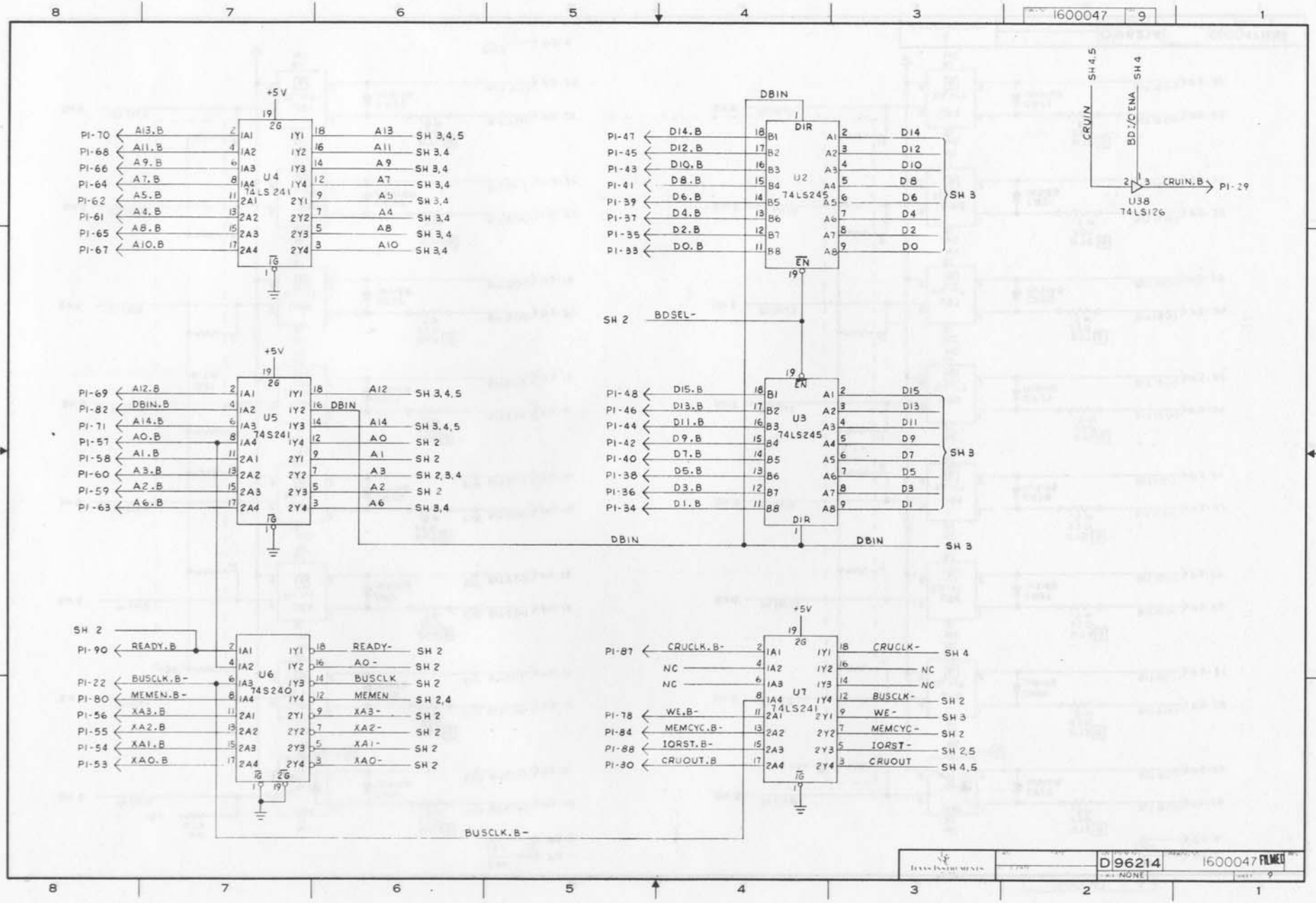

1600047 5
U44 5 DS1 TIL220 R101 330 +5V
7406 "STATUS 1"
IORST- PORST- SH 9 SH 4
U44 5 DS2 TIL220 R80 330 +5V
7406 "STATUS 2"
CRUOUT
SH 9 A14
A13
A12
SH 4 OUTSEL3-
U33 74LS259
MASK 0
MASK 1
MASK 2
MASK 3
NC
NC
INTRES-
SH 4 OUTSEL2-
74LS32
74LS02
74LS32
U32 74LS139
INTRST0-
INTRST1-
INTRST2-
INTRST3-
NC
NC
BDIORST-
74LS08
BDINTRST-
74LS08
A12
A13
A14
PIIN0/INT0
PIIN1/INT1
PIIN2/INT2
PIIN3/INT3
U42
SH 8 PIIN4
PIIN5
PIIN6
PIIN7
74LS251
SH 4 INSEL 2-
A12
A13
A14
PIIN15/BDINT
U40
SH 8 PIIN8
PIIN9
PIIN10
PIIN11
PIIN12
PIIN13
PIIN14
74LS251
SH 4 INSEL 3-
SH 9 CRUIN
E95 PIIN0
E94
E93 INT0
E92 PIIN1
E91
E90 INT1
E89 PIIN2
E88
E87 INT2
E86 PIIN3
E85
E84 INT3
E83
E82
E81 BDINT
SH 8 PIIN15 PIIN3 PIIN2 PIIN1 PIIN0
INTRST0-
INTRES-
PIINO
74LS08
74LS14
U34 74LS74
+5V
MASK 0
INT0-
INT0
MASK 1
INT1
MASK 2
INT2
MASK 3
INT3
INT1-
INT2-
INT3-
7406
INT4.B- PI-18
INT5.B- PI-17
INT6.B- PI-20
INT7.B- PI-6
LVL INT LVL
INT8.B- PI-5
INT9.B- PI-8
INT10.B- PI-7
INT11.B- PI-10
INT12.B- PI-9
INT13.B- PI-12
INT14.B- PI-11
INT15.B- PI-14
INT1.B- PI-16
INT2.B- PI-13
INT3.B- PI-15
BDINT-
74S260
BDINT
D96214
1600047 FILMED
NONE
5


1600047 6
PO IN 0
PO IN 1
PO IN 2
PO IN 3
PO IN 4
PO IN 5
PO IN 6
PO IN 7
PO OUT 0
PO OUT 1
PO OUT 2
PO OUT 3
PO OUT 4
PO OUT 5
PO OUT 6
PO OUT 7
BIT 0 (+)
BIT 0 (-)
BIT 1 (+)
BIT 1 (-)
BIT 2 (+)
BIT 2 (-)
BIT 3 (+)
BIT 3 (-)
BIT 4 (+)
BIT 4 (-)
BIT 5 (+)
BIT 5 (-)
BIT 6 (+)
BIT 6 (-)
BIT 7 (+)
BIT 7 (-)
+5V
+5VA
7406
TIL117
TIL119
IN914B
D96214
1600047 FILMED


1600047 7
R31 4.7K
+5V
SH 4
PO IN 8
U76
TIL117
CR9 IN914B
R56 220 .5W
R93 .5W
+5VA
BIT 8 (+)
P2-26
BIT 8(-)
P2-25
R30 220
U47
7406
PO OUT 8
U60
TIL119
R28 4.7K
PO IN 9
U77
TIL117
CR10 IN914B
R57 220 .5W
R94 .5W
BIT 9 (+)
P2-28
BIT 9(-)
P2-27
R29 220
PO OUT 9
U61
TIL119
R27 4.7K
PO IN 10
U78
TIL117
CR11 IN914B
R58 220 .5W
R95 .5W
BIT 10(+)
P2-30
BIT 10(-)
P2-29
R26 220
PO OUT 10
U62
TIL119
R24 4.7K
PO IN 11
U79
TIL117
CR12 IN914B
R59 220 .5W
R96 .5W
BIT 11(+)
P2-32
BIT 11(-)
P2-31
R25 220
PO OUT 11
U63
TIL119
R23 4.7K
PO IN 12
U80
TIL117
CR13 IN914B
R60 220 .5W
R97 .5W
BIT 12(+)
P2-34
BIT 12(-)
P2-33
R22 220
PO OUT 12
U64
TIL119
R20 4.7K
PO IN 13
U81
TIL117
CR14 IN914B
R61 220 .5W
R98 .5W
BIT 13(+)
P2-36
BIT 13(-)
P2-35
R21 220
PO OUT 13
U65
TIL119
R19 4.7K
PO IN 14
U82
TIL117
CR15 IN914B
R62 220 .5W
R99 .5W
BIT 14(+)
P2-38
BIT 14(-)
P2-37
R18 220
PO OUT 14
U66
TIL119
R16 4.7K
PO IN 15
U83
TIL117
CR16 IN914B
R63 220 .5W
R100 .5W
BIT 15(+)
P2-40
BIT 15(-)
P2-39
R17 220
PO OUT 15
U67
TIL119
NC
D96214
1600047 FILMED
NONE

C-8


1600047 8
R9 4.7K
+5V
SH 5
PIIN0
U84
TIL117
CR17 IN914B
R64 220 .5W
E113 BIT0(+)
E112 BIT0(-)
P3-10
P3-9
PIIN1
U85
CR18 IN914B
R65 220 .5W
E115 BIT1(+)
E114 BIT1(-)
P3-12
P3-11
PIIN2
U86
CR19 IN914B
R66 220 .5W
E116 BIT2(+)
E117 BIT2(-)
P3-14
P3-13
PIIN3
U87
CR20 IN914B
R67 220 .5W
E118 BIT3(+)
E119 BIT3(-)
P3-16
P3-15
PIIN4
U88
CR21 IN914B
R68 220 .5W
BIT4(+)
BIT4(-)
P3-18
P3-17
U41 4.7K
PIIN5
U89
CR22 IN914B
R69 220 .5W
BIT5(+)
BIT5(-)
P3-20
P3-19
PIIN6
U90
CR23 IN914B
R70 220 .5W
BIT6(+)
BIT6(-)
P3-22
P3-21
PIIN7
U91
CR24 IN914B
R71 220 .5W
BIT7(+)
BIT7(-)
P3-24
P3-23
E96
E97
E103
P3-1
P3-2
P3-8
PIIN8
U92
CR25 IN914B
R72 220 .5W
BIT8(+)
BIT8(-)
P3-26
P3-25
PIIN9
U93
CR26 IN914B
R73 220 .5W
BIT9(+)
BIT9(-)
P3-28
P3-27
PIIN10
U94
CR27 IN914B
R74 220 .5W
BIT10(+)
BIT10(-)
P3-30
P3-29
PIIN11
U95
CR28 IN914B
R75 220 .5W
BIT11(+)
BIT11(-)
P3-32
P3-31
PIIN12
U96
CR29 IN914B
R76 220 .5W
BIT12(+)
BIT12(-)
P3-34
P3-33
PIIN13
U97
CR30 IN914B
R77 220 .5W
BIT13(+)
BIT13(-)
P3-36
P3-35
PIIN14
U98
CR31 IN914B
R78 220 .5W
BIT14(+)
BIT14(-)
P3-38
P3-37
PIIN15
U99
CR22 IN914B
R79 220 .5W
BIT15(+)
BIT15(-)
P3-40
P3-39
E99
E101
P3-4
P3-6
D 96214
1600047 FILMED


+5V
U4
74LS241
PI-70 AI3.B
PI-68 AII.B
PI-66 A9.B
PI-64 A7.B
PI-62 A5.B
PI-61 A4.B
PI-65 A8.B
PI-67 AIO.B
SH 3,4,5
SH 3,4
SH 3,4
SH 3,4
SH 3,4
SH 3,4
SH 3,4
SH 3,4
DBIN
U2
74LS245
PI-47 DI4.B
PI-45 DI2.B
PI-43 DIO.B
PI-41 D8.B
PI-39 D6.B
PI-37 D4.B
PI-35 D2.B
PI-33 DO.B
D14
D12
DIO
D8
D6
D4
D2
DO
SH 3
SH 2 BDSEL-
U5
74S241
PI-69 AI2.B
PI-82 DBIN.B
PI-71 AI4.B
PI-57 AO.B
PI-58 AI.B
PI-60 A3.B
PI-59 A2.B
PI-63 A6.B
SH 3,4,5
SH 3,4,5
SH 2
SH 2
SH 2,3,4
SH 2
SH 3,4
U3
74LS245
PI-48 DI5.B
PI-46 DI3.B
PI-44 DII.B
PI-42 D9.B
PI-40 D7.B
PI-38 D5.B
PI-36 D3.B
PI-34 DI.B
DI5
DI3
DII
D9
D7
D5
D3
DI
SH 3
DBIN
DBIN
SH 3
U6
74S240
SH 2
PI-90 READY.B
PI-22 BUSCLK.B-
PI-80 MEMEN.B-
PI-56 XA3.B
PI-55 XA2.B
PI-54 XAI.B
PI-53 XAO.B
READY-
AO-
BUSCLK
MEMEN
XA3-
XA2-
XAI-
XAO-
SH 2
SH 2
SH 2
SH 2,4
SH 2
SH 2
SH 2
SH 2
U7
74LS241
+5V
PI-87 CRUCLK.B-
NC
NC
PI-78 WE.B-
PI-84 MEMCYC.B-
PI-88 IORST.B-
PI-30 CRUOUT.B
CRUCLK-
NC
NC
BUSCLK-
WE-
MEMCYC-
IORST-
CRUOUT
SH 4
SH 2
SH 3
SH 2
SH 2,5
SH 4,5
BUSCLK.B-
SH 4.5
SH 4
CRUIN
BDJCENA
CRUIN.B
PI-29
U38
74LS126

APPENDIX D

CHASSIS INTERFACE CONNECTOR (P1) SIGNAL ASSIGNMENTS

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
33	D0.B	63	A6.B	5	INT8.B
34	D1.B	64	A7.B	8	INT9.B
35	D2.B	65	A8.B	7	INT10.B
36	D3.B	66	A9.B	10	INT11.B
37	D4.B	67	A10.B	9	INT12.B
38	D5.B	68	A11.B	12	INT13.B
39	D6.B	69	A12.B	11	INT14.B
40	D7.B	70	A13.B	14	INT15.B
41	D8.B	71	A14.B	75	+12V
42	D9.B	22	BUSCLK.B-	76	+12V
43	D10.B	80	MEMEN.B-	3	+5V
44	D11.B	84	MEMCYC.B-	4	+5V
45	D12.B	90	READY.B	97	+5V
46	D13.B	82	DBIN.B	98	+5V
47	D14.B	78	WE.B-	1	GND
48	D15.B	29	CRUIN.B	2	GND
53	XA0.B	30	CRUOUT.B	77	GND
54	XA1.B	87	CRUCLK.B-	79	GND
55	XA2.B	88	IORST.B-	81	GND
56	XA3.B	16	INT1.B-	83	GND
57	A0.B	13	INT2.B-	85	GND
58	A1.B	15	INT3.B-	89	GND
59	A2.B	18	INT4.B-	91	GND
60	A3.B	17	INT5.B-	99	GND
61	A4.B	20	INT6.B-	100	GND
62	A5.B	6	INT7.B-		

NOTE

This table lists only those signals of the TM990 bus which this board uses.

APPENDIX E

EDGE CONNECTOR (P2,P3) PIN ASSIGNMENTS

PIN	SIGNAL	PIN	SIGNAL
1	RESERVED	2	RESERVED
3	+5 V	4	+8 V*
5	GROUND	6	RESERVED
7	GROUND	8	RESERVED
9	BIT 0 (-)	10	BIT 0 (+)
11	BIT 1 (-)	12	BIT 1 (+)
13	BIT 2 (-)	14	BIT 2 (+)
15	BIT 3 (-)	16	BIT 3 (+)
17	BIT 4 (-)	18	BIT 4 (+)
19	BIT 5 (-)	20	BIT 5 (+)
21	BIT 6 (-)	22	BIT 6 (+)
23	BIT 7 (-)	24	BIT 7 (+)
25	BIT 8 (-)	26	BIT 8 (+)
27	BIT 9 (-)	28	BIT 9 (+)
29	BIT 10 (-)	30	BIT 10 (+)
31	BIT 11 (-)	32	BIT 11 (+)
33	BIT 12 (-)	34	BIT 12 (+)
35	BIT 13 (-)	36	BIT 13 (+)
37	BIT 14 (-)	38	BIT 14 (+)
39	BIT 15 (-)	40	BIT 15 (+)

*P2 only

APPENDIX F

5MT INTERFACE

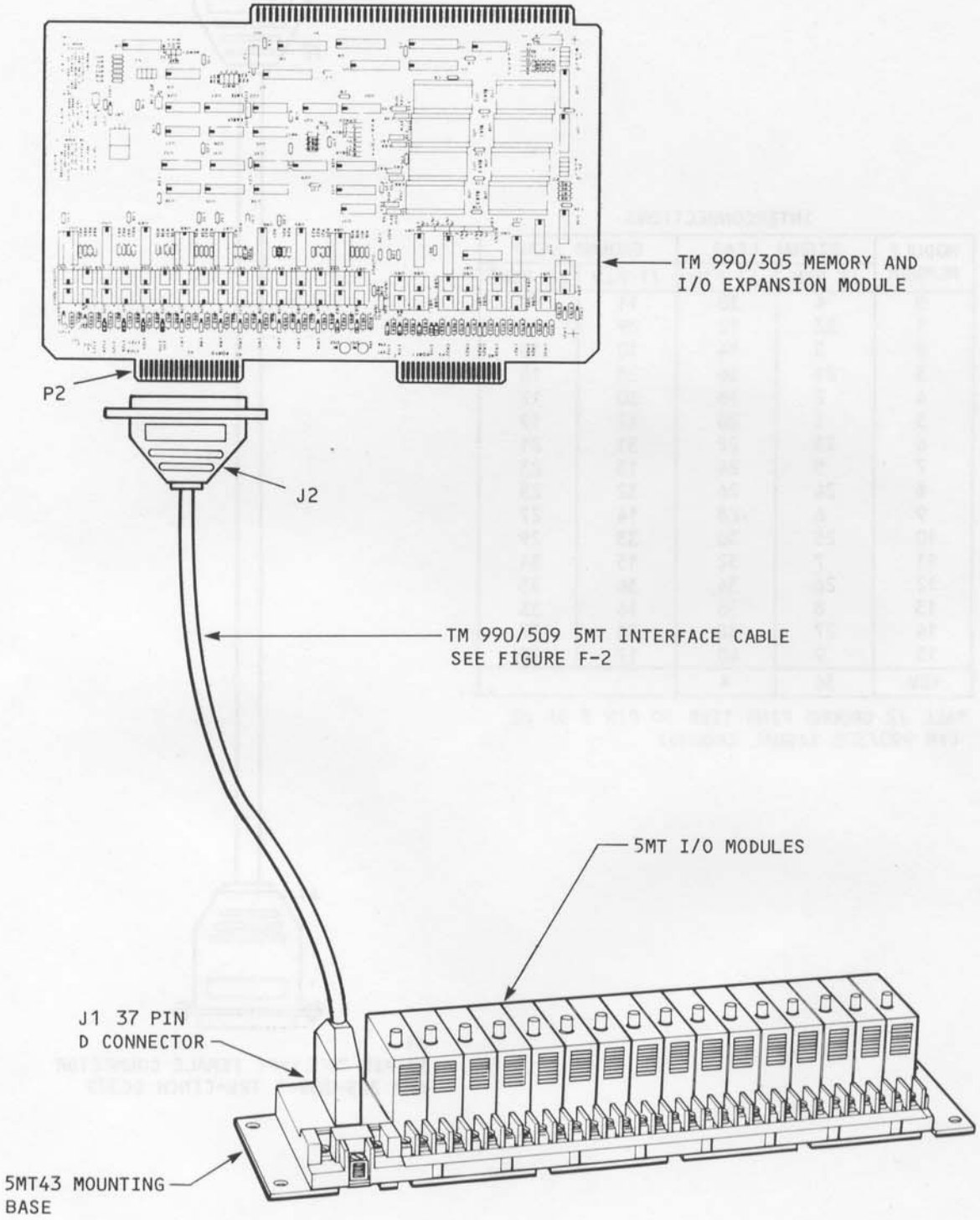


FIGURE F-1. TM 990/305 TO 5MT INTERCONNECTION

INTERCONNECTIONS

MODULE MUMBER	SIGNAL LEAD		GROUND LEAD	
	J1 PIN	J2 PIN	J1 PIN	J2 PIN*
0	4	10	11	9
1	22	12	29	11
2	3	14	10	13
3	21	16	28	15
4	2	18	30	17
5	1	20	12	19
6	23	22	31	21
7	5	24	13	23
8	24	26	32	25
9	6	28	14	27
10	25	30	33	29
11	7	32	15	31
12	26	34	34	33
13	8	36	16	35
14	27	38	35	37
15	9	40	17	39
+8V	36	4		

*ALL J2 GROUND PINS TIED TO PIN 7 OF J2
(TM 990/305 SIGNAL GROUND)

FIGURE F-2. TM 990/509 5MT INTERFACE CABLE

APPENDIX G

TMS 4016 DATA SHEET

MOS LSI

TMS 4016 JL, JDL, NL
2048-WORD BY 8-BIT STATIC RAM

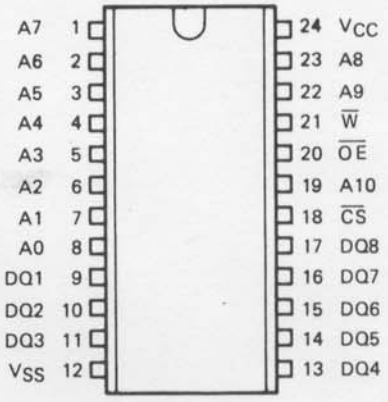
NOVEMBER 1978

- **2K × 8 Organization**
- **Single +5 V Supply (10% Tolerance)**
- **Fully Static Operation (No Clocks, No Refresh)**
- **JEDEC Proposed Standard Pinout**
- **24-Pin 600 Mil (15.2 mm) Package Configuration**
- **Plug-in Compatible with 16K 5V EPROMs**
- **8-Bit Output for Use in Microprocessor-Based Systems**
- **Performance Ranges**

	Max Access/Min Cycle
— TMS 4016-25	250 ns
— TMS 4016-20	200 ns
— TMS 4016-15	150 ns

- **Tri-State Outputs with $\overline{CS}$ for OR-ties**
- **$\overline{OE}$ Eliminates Need for External Bus Buffers**
- **Common I/O Capability**
- **All Inputs and Outputs Fully TTL Compatible**
- **Fanout to Series 74, Series 74S, or Series 74LS TTL Loads**
- **N-Channel Silicon-Gate Technology**
- **Power Dissipation Under 495 mW Max**
- **Guaranteed dc Noise Immunity of 400 mV with Standard TTL Loads**

TMS 4016
24-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A10	Addresses
DQ1-DQ8	Data In/Data Out
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{W}$	Write Enable
V_{SS}	Ground
V_{CC}	+5 V Supply

description

The TMS 4016 static random-access memory is organized as 2048 words of 8 bits each. Fabricated using proven N-channel, silicon-gate MOS technology, the TMS 4016 operates at high speeds and draws less power per bit than 4K static RAMs. It is fully compatible with Series 74, 74S, or 74LS TTL. Its static design means that no refresh clocking circuitry is needed and timing requirements are simplified. Access time is equal to cycle time. A chip select control is provided for controlling the flow of data-in and data-out and an output enable function is included in order to eliminate the need for external bus buffers.

Of special importance is that the TMS 4016 static RAM has the same standardized pinout as TI's compatible EPROM family. This, along with other compatible features, makes the TMS 4016 directly plug-in compatible with the TMS 2516 (or other 16K 5V EPROMs). No modifications are needed. This allows the microprocessor sytem designer complete flexibility in partitioning his memory board between read/write and non-volatile storage.

ADVANCED INFORMATION:
Complete data sheet will be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

APPENDIX H

TMS 2516 AND TMS 2532 DATA SHEETS

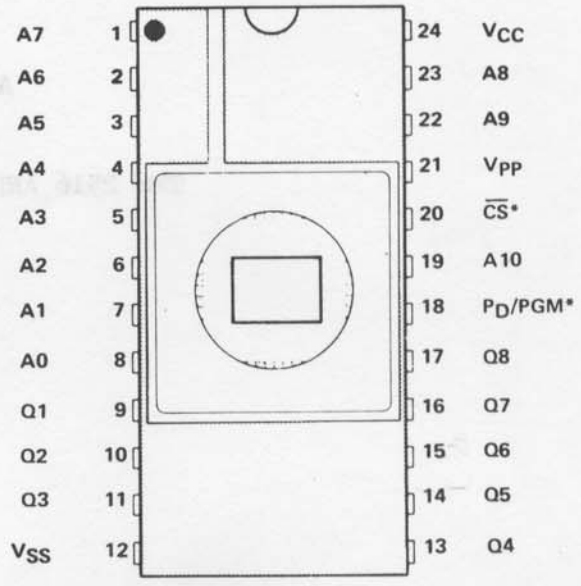
MOS LSI

TMS 2516 JL AND TMS 2532 JL 16K AND 32K EPROMs

APRIL 1978

- Organization:
  - TMS 2516 . . . 2K X 8
  - TMS 2532 . . . 4K X 8
- Single +5 V Power Supply
- Pin Compatible with Existing ROMs and EPROMs (8 K, 16 K, 32 K, and 64 K)
- JEDEC Standard Pinouts
- All Inputs/Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Max Access/Min Cycle Time . . . 450 ns
- 8-Bit Output for Use in Microprocessor-Based Systems
- N-Channel Silicon-Gate Technology
- 3-State Output Buffers
- Low Power
  - Active:
    - TMS 2516 . . . 285 mW Typical
    - TMS 2532 . . . 400 mW Typical
  - Standby . . . 50 mW Typical
- Guaranteed dc Noise Immunity with Standard TTL Loads
- No Pull-Up Resistors Required

TMS 2516
24-PIN CERAMIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



*FOR TMS 2532:
PIN 18 . . . A11
PIN 20 . . . PD/$\overline{PGM}$

PIN NOMENCLATURE	
A(N)	Address inputs
$\overline{CS}$	Chip Select
PD/PGM, PD/$\overline{PGM}$	Power Down/Program
Q(N)	Input/Output
V_{CC}	+5 V Power Supply
V_{PP}	+25 V Power Supply
V_{SS}	0 V Ground

description

The TMS 2516 JL and TMS 2532 JL are 16,384-bit and 32,768-bit, untraviolet light erasable, electrically programmable read-only memories. These devices are fabricated using N-channel silicon-gate technology for high speed and simple interface with MOS and Bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for OR-tying multiple devices on a common bus. The TMS 2516 is upward pin-compatible with the TMS 2532 and the TMS 2532 is plug-in compatible with the TMS 4732 32K ROM.

Since these EPROMs operate from a single +5 V supply (in the read mode), they are ideal for use in microprocessor systems. One other (+25 V) supply is needed for programming but all programming signals are TTL level, requiring a single 50 ms pulse. For programming outside of the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random. Total programming time for all bits for the TMS 2516 is 100 seconds; 200 seconds for the TMS 2532.

operation

DEVICE		MODE										
FUNCTION (PINS)		Read		Output Disable		Power Down		Start Programming		Inhibit Programming		Program Verification
TMS 2516	TMS 2532	TMS 2516	TMS 2532	TMS 2516	TMS 2532	TMS 2516	TMS 2532	TMS 2516	TMS 2532	TMS 2516	TMS 2532	TMS 2516
PD/PGM (18)	PD/$\overline{PGM}$ (20)	V_{IL}	V_{IL}	Don't Care	V_{IH}	V_{IH}	V_{IH}	Pulsed V_{IL} to V_{IH}	Pulsed V_{IH} to V_{IL}	V_{IL}	V_{IH}	V_{IL}
$\overline{CS}$ (20)	Use PD/$\overline{PGM}$ as chip select	V_{IL}	N/A	V_{IH}	N/A	Don't Care	N A	V_{IH}	N A	V_{IH}	N A	V_{IL}
V_{PP} (21)	V_{PP} (21)	+5	+5	+5	+5	+5	+ 5	+25	+25	+25	+25	+25 (or + 5)
V_{CC} (24)	V_{CC} (24)	+5	+5	+5	+5	+5	+5	+5	+5	+5	+5	+5
Q (9 to 11, 13 to 17)	Q (9 to 11, 13 to 17)	Q	Q	HI-Z	HI-Z	HI-Z	HI-Z	D	D	HI-Z	HI-Z	Q

read/output disable

When the outputs of two or more TMS 2516's and/or TMS 2532's are commoned on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. If the device whose output is to be read is a TMS 2516, it should have a low-level TTL signal applied to the $\overline{CS}$ and PD/PGM pins. If it is a TMS 2532, the low-level signal is applied to the PD/$\overline{PGM}$ pin. All other devices in the circuit should have their outputs disabled by applying a high-level signal to these same pins. (PD/PGM on the TMS 2516, can be left low, but it may be advantageous to power down the device during output disable.) Output data is accessed at pins Q1 to Q8. Data can be accessed in 450 ns = $t_{a(A)}$. (On the TMS 2516 access time from $\overline{CS}$ is 150 ns = $t_{a(\overline{CS})}$, once the addresses are stable.)

power down

Active power dissipation can be cut by 80% by applying a high TTL signal to the PD/PGM (PD/$\overline{PGM}$ for the TMS 2532) pin. In this mode all outputs are in a high-impedance state.

erasure

Before programming, the TMS 2516 or TMS 2532 is erased by exposing the chip through the transparent lid to high intensity untraviolet light (wavelength 2537 angstroms). The recommended minimum exposure does (= UV intensity X exposure time) is fifteen watt-seconds per square centimeter. A typical 12 milliwatt per square centimeter, filterless UV lamp will erase the device in about 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the "1" state.

start programming

After erasure (all bits in logic "1" state), logic "0's" are programmed into the desired locations. A "0"' can be erased only by ultraviolet light. The programming mode is achieved when V_{PP} is 25 V and $\overline{CS}$ (for TMS 2516 only) is at V_{IN}. Data is presented in parallel (8 bits) on pins Q1 to Q8. Once addresses and data are stable, a 50 millisecond high TTL pulse (low for the TMS 2532) should be applied to the PGM pin at each address location to be programmed. Maximum pulse width is 55 milliseconds. Locations can be programmed in any order. More than one TMS 2516 or TMS 2532 can be programmed when the devices are connected in parallel.

inhibit programming

When two or more devices (either TMS 2516 or TMS 2532, or a combination of both) are connected in parallel, data can be programmed into all devices or only chosen devices. TMS 2516's not intended to be programmed (i.e., inhibited) should have a low level applied to the PD/PGM pin and a high-level applied to the $\overline{CS}$ pin. TMS 2532's not intended to be programmed should have a high level applied to PD/$\overline{PGM}$.

program verification

A verify is done to see if the device was programmed correctly. A verify can be done at any time. It can be done on each location immediately after that location ia programmed. To do a verify on the TMS 2516 Vpp may be kept at + 25 V. (Verify on the TMS 2532 is the read operation.)

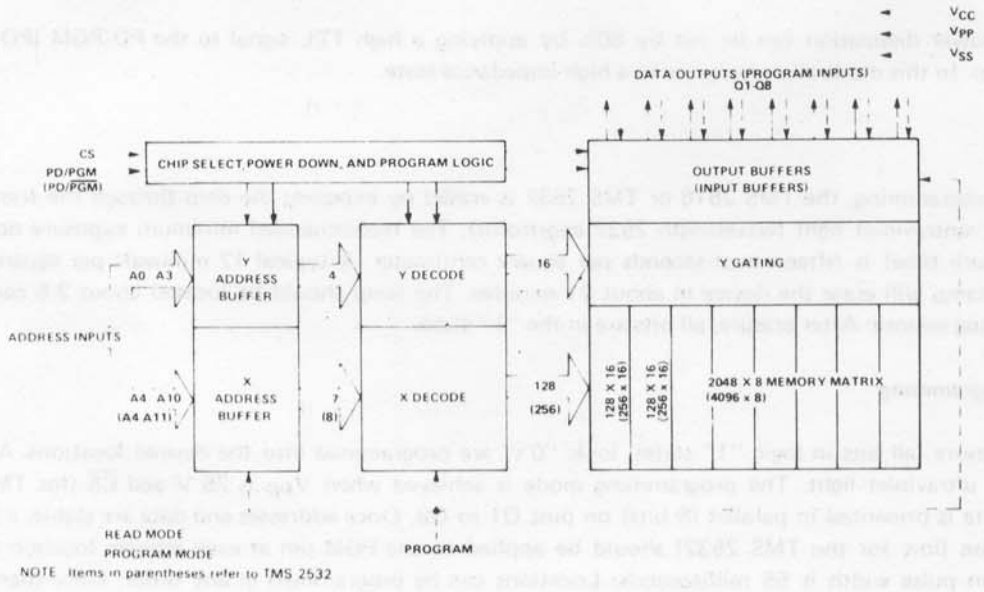
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1)	−0.3 to 6 V
Supply voltage, V_{PP} (see Note 1)	−0.3 to 28 V
All input voltages (see Note 1)	−0.3 to 6 V
Output voltage (operating with respect to V_{SS})	−0.3 to 6 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 125°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{SS} (substrate).

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

functional block diagram



recommended operating conditions

PARAMETER	TMS 2516			TMS 2532			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 2)	4.75	5	5.25	4.75	5	5.25	V
Supply voltage, V_{PP} (see Note 3)	V_{CC}–0.6	V_{CC}	V_{CC}+0.6	V_{CC}–0.6	V_{CC}	V_{CC}+0.6	V
Supply voltage, V_{SS}		0			0		V
High-level input voltage, V_{IH}	2.0		V_{CC}+1	2.2		V_{CC}+1	V
Low-level input voltage, V_{IL}	–0.1		0.8	–0.1		0.65	V
Read cycle time, $t_{c(rd)}$	450			450			ns
Operating free-air temperature, T_A	0		70	0		70	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} is applied so that the device is not damaged.

3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. Tolerance of ± .6 volts enables the V_{PP} pin to be switched from V_{CC} (read) to 25 volts (programming) using a drive circuit. During programming, V_{PP} must be maintained at 25V (± 1V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER			TEST CONDITIONS	TMS 2516			TMS 2532			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage		I_{OH} = –400 μA	2.4			2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.45			0.45	V
I_I	Input current (leakage)		V_I = 5.25V			10			10	μA
I_O	Output current (leakage)		V_O = 5.25V			10			10	μA
I_{PP1}	V_{PP} supply current	TMS 2516	V_{PP} = 5.85V, PD/PGM = V_{IL}			6			12	mA
		TMS 2532	V_{PP} = 5.85V, PD/$\overline{PGM}$ = V_{IL}							
I_{PP2}	V_{PP} supply current (during program pulse)	TMS 2516	PD/PGM = V_{IH}			30			30	mA
		TMS 2532	PD/$\overline{PGM}$ = V_{IL}							
I_{CC1}	V_{CC} supply current (standby)	TMS 2516	PD/PGM = V_{IH}		10	25		10	25	mA
		TMS 2532	PD/$\overline{PGM}$ = V_{IH}							
I_{CC2}	V_{CC} supply current (active)	TMS 2516	$\overline{CS}$ = PD/PGM = V_{IL}		57	100		80	160	mA
		TMS 2532	PD/$\overline{PGM}$ = V_{IL}							

†Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended supply voltage and operating free-air temperature range
f = 1 MHz

PARAMETER		TEST CONDITIONS	TYP†	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz	4	6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	8	12	pF

†All typical values are T_A = 25°C and nominal voltage.

switching characteristics over full ranges of recommended operating conditions, (unless otherwise noted)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	MIN	TYP†	MAX	UNIT
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, $t_r \leqslant 20$ ns, $t_f \leqslant 20$ ns		280	450	ns
$t_{a(\overline{CS})}$	Access time from chip select (TMS 2516 only)				150	ns
$t_{a(PR)}$	Access time from PD/PGM (PD/$\overline{PGM}$ for TMS 2532)			280	450	ns
t_{PVX}	Output not valid from address change		0			ns
t_{PXZ}	Output disable time from chip deselect during read only		0		100	ns
t_{PXZ}	Output disable time from chip deselect during program and program verify				120	ns
t_{PXZ}	Output disable time from PD/PGM (PD/$\overline{PGM}$ for TMS 2532) during standby		0		100	ns

†All typical values are at T_A = 25°C and nominal voltages.

recommended timing requirements for programming T_A = 25°C (see Note 4)

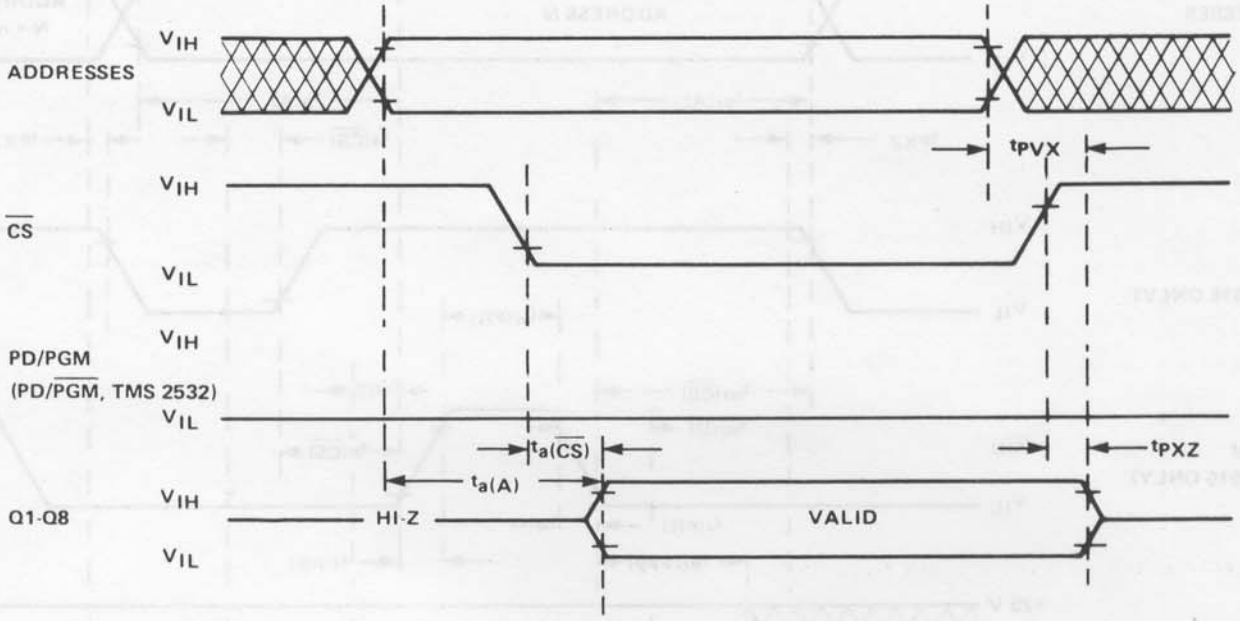
PARAMETER		MIN	TYP†	MAX	UNIT
$t_{w(PR)}$	Pulse width, program pulse	45	50	55	ms
$t_{r(PR)}$	Rise time, program pulse	5			ns
$t_{f(PR)}$	Fall time, program pulse	5			ns
$t_{su(A)}$	Address setup time	2			μs
$t_{su(\overline{CS})}$	Chip-select setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(Vpp)}$	Setup time from Vpp	0			ns
$t_{h(A)}$	Address hold time	2			μs
$t_{h(\overline{CS})}$	Chip-select hold time (TMS 2516 only)	2			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{h(PR)}$	Program pulse hold time (TMS 2532 only)	0			ns
$t_{h(Vpp)}$	Vpp hold time (TMS 2532 only)	0			ns

†Typical values are at nominal voltages.

NOTES: 4. For all switching characteristics and timing measurements, input pulse levels are 0.65 V to 2.2 V and Vpp = 25 V ± 1 V during programming.

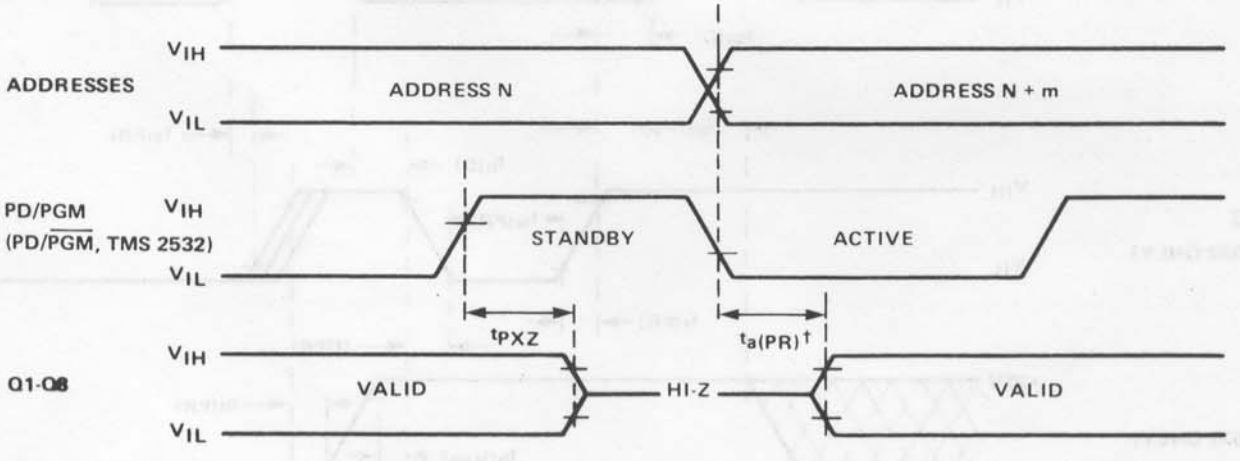
5. Common test conditions apply for t_{PXZ} except during programming. For $t_{a(A)}$, $t_{a(\overline{CS})}$, and t_{PXZ}, PD/PGM = $\overline{CS}$ = V_{IL} for the TMS 2516 and PD/$\overline{PGM}$ = V_{IL} for the TMS 2532.

read cycle timing



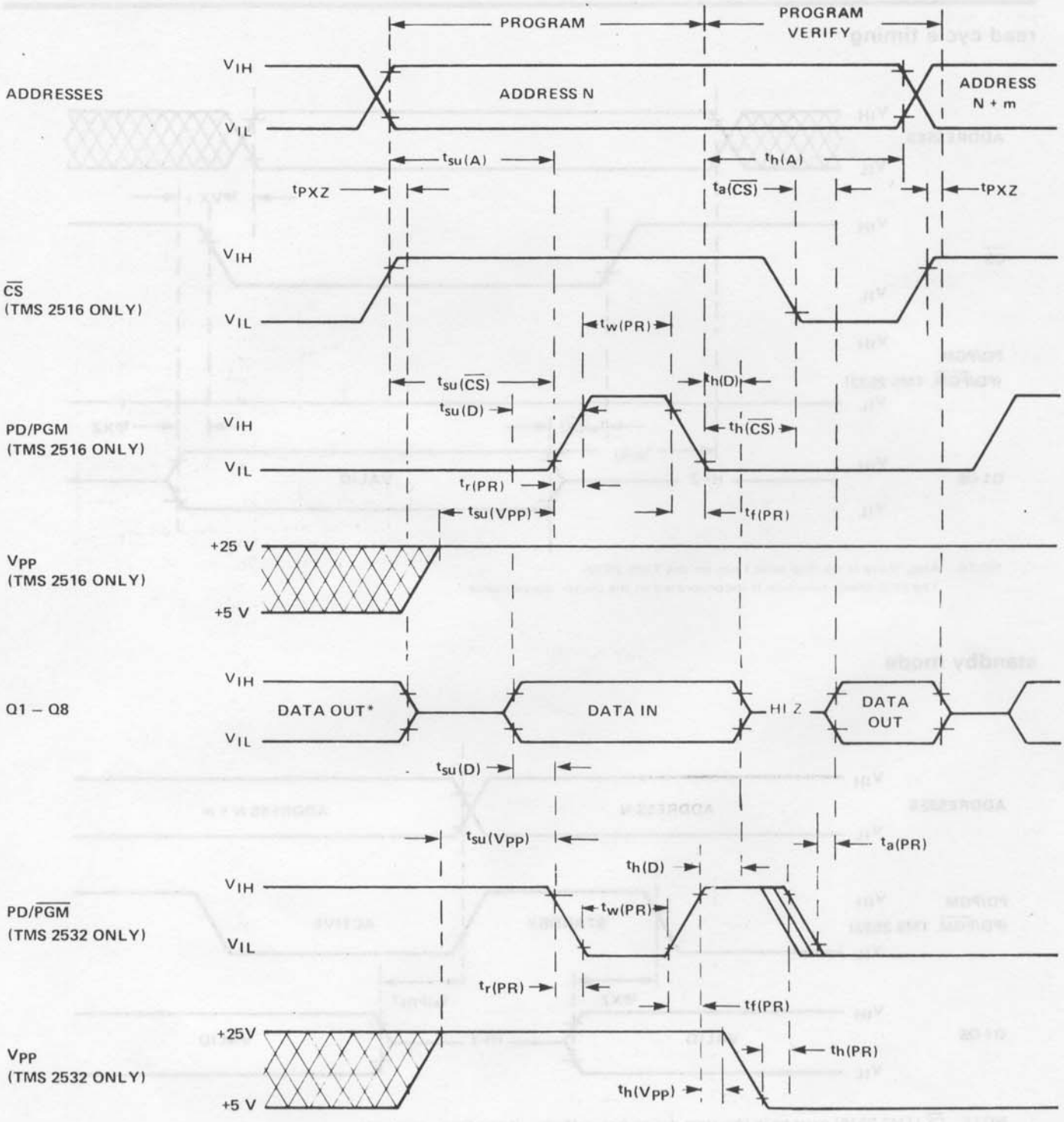
NOTE: Also, there is no chip select pin on the TMS 2532.
The chip-select function is incorporated in the power down mode.

standby mode



NOTE: $\overline{CS}$ (TMS 2516) must be in low state during Active Mode, "Don't Care" otherwise.
† $t_{a(PR)}$ referenced to PD/PGM (PD/$\overline{PGM}$ for TMS 2532) or the address, whichever occurs last.

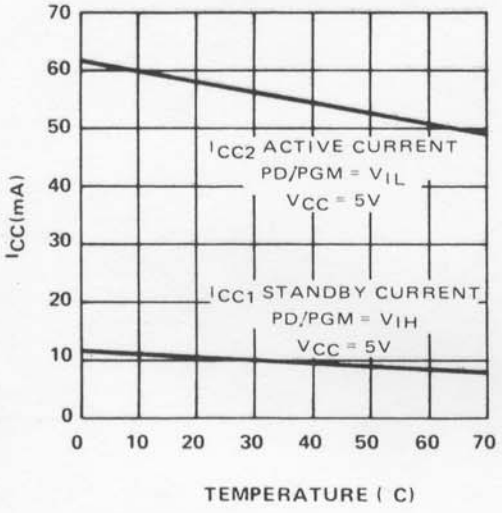
program cycle timing



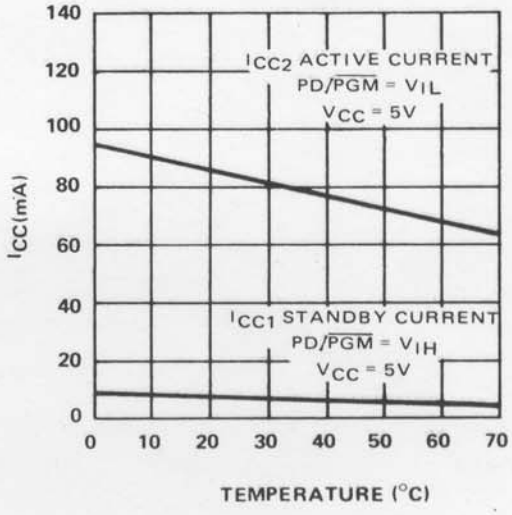
NOTE: There is no chip select function for the TMS 2532.
$\overline{CS}$ (TMS 2516) is in "don't care" state.
*HI Z for the TMS 2532.

typical device characteristics (read mode)

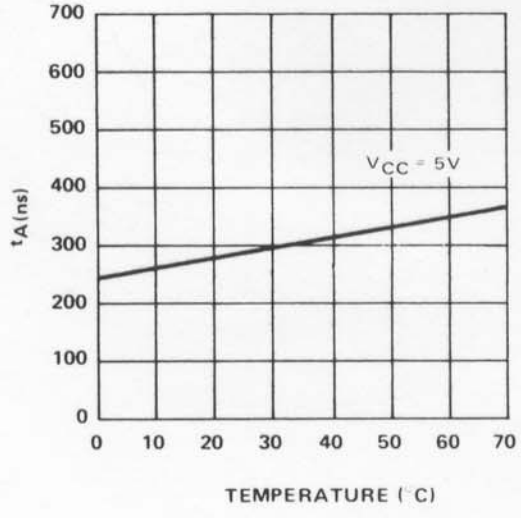
TMS 2516
I_{CC} CURRENT
vs.
TEMPERATURE



TMS 2532
I_{CC} CURRENT
vs.
TEMPERATURE



TMS 2516 and TMS 2532
ACCESS TIME
vs.
TEMPERATURE



TM 990/305 COMBINATION MEMORY AND I/O EXPANSION MODULE USER'S GUIDE

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Comments:_____

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