TEXAS INSTRUMENTS

TM 990

TM 990/302
Hardware User's Guide

MICROPROCESSOR SERIES™

July 1980

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TABLE OF CONTENTS

APPENDICES

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION I

INTRODUCTION

1.1 GENERAL

The TM 990/302 software development board is designed around the TM 990/10X series of microcomputers. It is intended for use as a low cost software development system with EPROM programming capabilities. Software development includes entering assembly language programs, program editing, assembling and debugging. Programming of EPROMS with the finished software is then accomplished using the EPROM programmer portion of the TM 990/302. The finished software in EPROM affords transportability and allows use of this end product in systems other than the TM 990 product line. The TM 990/302 software development board and its principle components are shown in Figure 1-1. The TM 990/302 is available with one software package, see Table 1-1.

TABLE 1-1. TM 990/302 PRODUCT MATRIX

MODEL	PRODUCT DESCRIPTION
TM 990/302-1	TM 990/302 software development board with TM 990/302 software development software package

Features of the TM 990/302 include:

- 2K words of TMS 4045 static RAM memory
- Flexible memory area allowing use of: TMS 2508 1K × 8 bits each
TMS 2516 2K × 8 bits each
TMS 2532 4K × 8 bits each
TMS 2716 2K × 8 bits each
- Variable address mapping for different memory configurations
- Dual audio cassette recorder interface with motor start/stop control
- EPROM programming with interchangeable EPROM personality programming cards (all programming signals are brought out on a 50 pin board edge connector for easy user interface)
- Programmable load logic for systems requiring a load on reset
- Programmable wait logic for use of slower low cost memories

1.2 PURPOSE AND SCOPE OF THE TM 990/302

The TMS 990/302 was developed to provide a low cost development tool for generating and testing software for the TMS 990/10X series of microcomputers. For operation, the software development board can be installed in the TM 990/510 chassis along with the microcomputer. This arrangement facilitates communications between the microprocessor and the board. In addition, supply voltages are routed to the board via the 510 chassis backplane. The software development system also calls for the use of low cost cassette recorders as a temporary storage medium for source/object files.

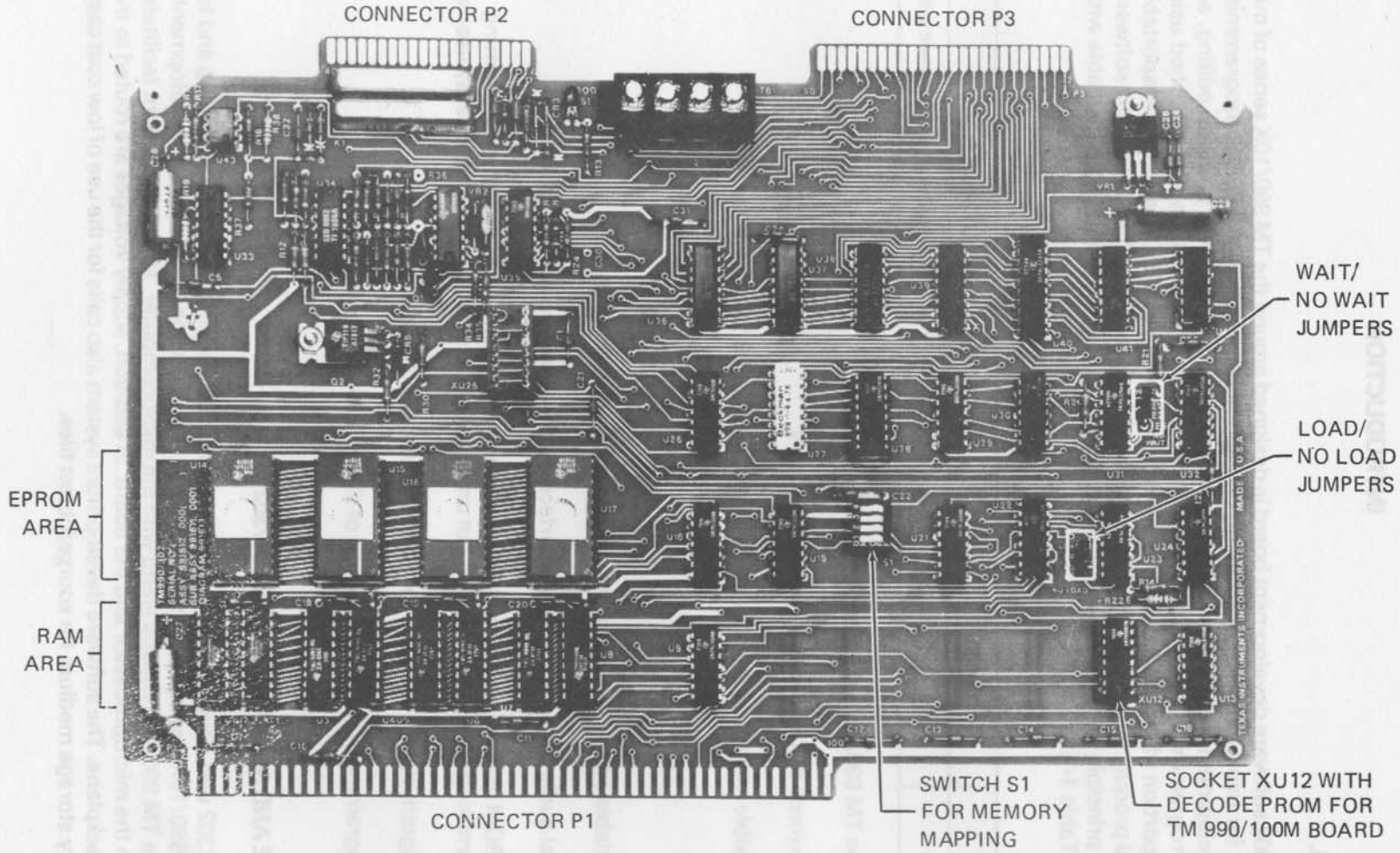


Figure 1-1. TM 990/302 Board

1.3 MANUAL ORGANIZATION

This manual is organized as follows:

- Section 1 contains an introduction to the TM 990/302
- Section 2 describes the installation and operation of the TM 990/302 board in a TM 990 microcomputer system including custom memory mapping.
- Section 3 presents an overview of the system and the theory of operation for the three main sections
- Appendices provide supplementary information

1.4 SPECIFICATIONS

- Voltage requirement: +12 V, −12 V, +5 V (+/−5%), and 35 −55 V unregulated
- Current requirement: +12 V (132 mA), −12 V (55 mA), +5 V (825 mA), and 35 −55 V unregulated (80 mA)
- Board dimensions: 19.05 cm by 27.94 cm (7.5 in. by 11 in.)
- Temperature range: Operating 0°C to 55°C
  Storage −40°C to 70°C
- Clock rate: The TMS 990/302 software development board can be operated at frequencies up to 4 MHz

1.5 APPLICABLE DOCUMENTS

The following is a list of documents that provides supplementary information for the TM 990/302 user.

- TM 990/100 Microcomputer User's Guide
- TMS 9900 Microprocessor Data Manual
- TM 990/302 Software Development Board User's Guide
- TM 990/514/515 EPROM Personality Module User's Guide

SECTION 2

INSTALLATION AND OPERATION

2.1 GENERAL

This section provides installation and operation instructions for the TM 990/302. Included topics are initial inspection, preparation for use, system configuration, and an example application. This section also explains how to custom configure the memory mapping on the TM 990/302 board.

2.2 INITIAL INSPECTION

Inspect the shipping container for damage. If the shipping container or package material is damaged, it should be kept until the board's performance has been verified. After removing the board from its carton, remove the protective packing carefully. Check the board for any abnormalities that could have incurred in shipping — report any discrepancies to your supplier.

2.3 EQUIPMENT

2.3.1 Required Equipment

A minimum system would consist of the following items:

- TM 990/510 or TM 990/520 card cage
- TM 990/518 power supply or equivalent (see paragraph 1.4 for power requirements)
- Terminal (see paragraph 2.3.2)
- TM 990/100 or TM 990/101 microcomputer board
- TM 990/5XX EPROM personality programming cards
- Audio cassette record player/players (see paragraph 2.3.2)

2.3.2 Recommended Equipment

The following is a list of recommended equipment:

- Terminals: Decwriter II
  Hazeltine 1500 Series
  Lear Siegler ADM-1, ADM-2, or ADM-3
  Soroc IQ 120
  Teletype Model 3320 5JE
  Texas Instruments Silent 733 KSR
  Texas Instruments Silent 743 KSR
- Audio Cassette Recorder/Players: General Electric 3-5121B
  Panasonic RQ-413 AS
  Realistic CTR-40
  Realistic CTR-41
  Sears 799-21683700
  Sharp RD 610

CAUTION

The TM990/302 audio cassette interface is not compatible with certain models of audio cassette recorder/players. Reliable operation is only warranted with the above audio cassette models. Operation with other models may not yield reliable data transfers and certain models of audio cassette units can damage the TM 990/302 control relay due to excesive inrush currents. Use of the TM 990/302 with other than the above listed audio cassette units voids factory warranty.

Criterion for selection of audio cassette recorder:
- UL approved
- Ear, aux, and remote inputs
- Volume control
- AC operation
- Stable motor speed

- Tape: Use any high quality digital or audio tapes of 60 minutes duration or less. Certified digital tapes are recommended.

2.4 CONNECT POWER SUPPLY

Connect the TM 990/518 power supply to the TM 990/5XX card cage as shown in Figure 2-1 (a). Verify correct voltages at the chassis rear panel connections before installing any boards into the chassis. There are two alternate ways to attach EPROM programming power to the TM 990/302 board. Attach the 35 V to 55 V EPROM power at the power supply terminal or at connector P2 as follows:

- At the power supply terminal on the TM 990/302 board, attach (see Figure 2-1 (b):
  1. TB1-1 to ground
  2. TB1-2 to voltage source
  3. TB1-3 and TB1-4 are unconnected.

- Or, at connector P2, attach (see Figure 2-1 (c):
  1. Pin 20 to voltage source
  2. Pins 1, 3, 5, or 7 to ground.

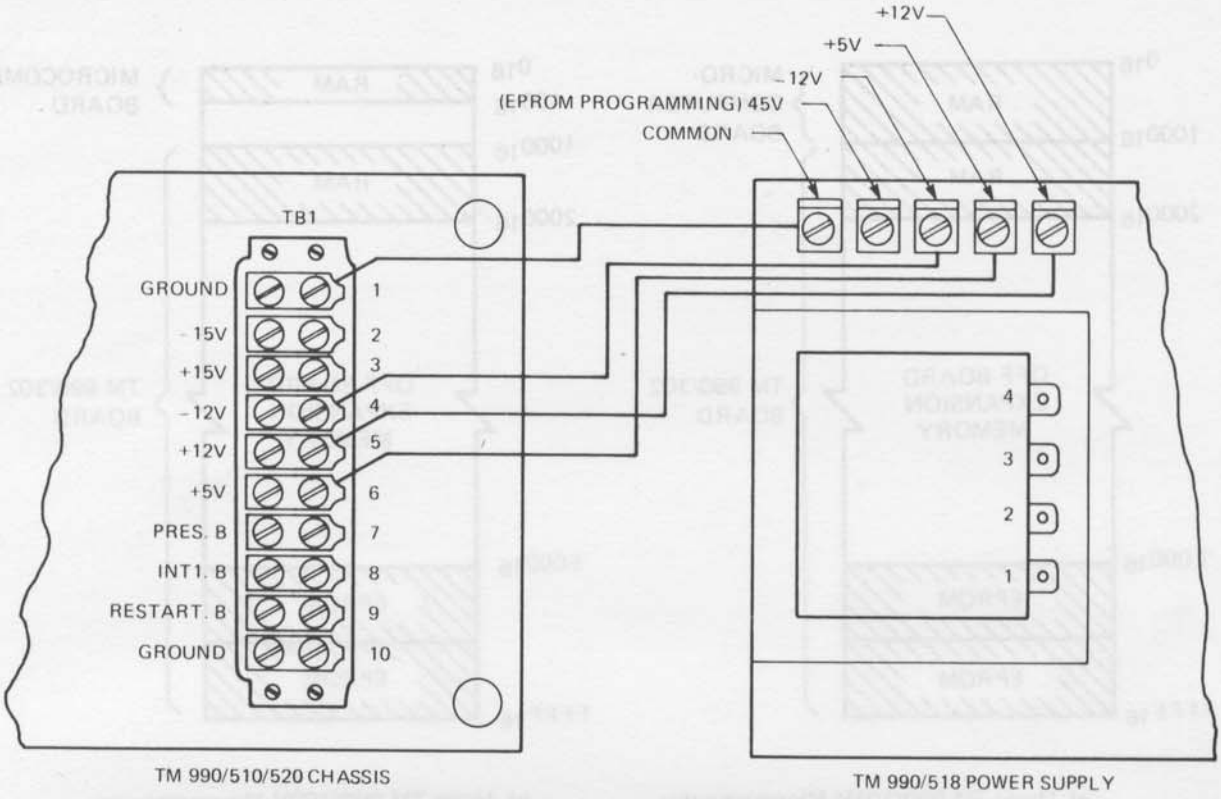
The EPROM power need not be connected if the EPROM programmer is not going to be used. See caution on page 2-20.

2.5 SET UP AND INSTALL MICROCOMPUTER BOARDS

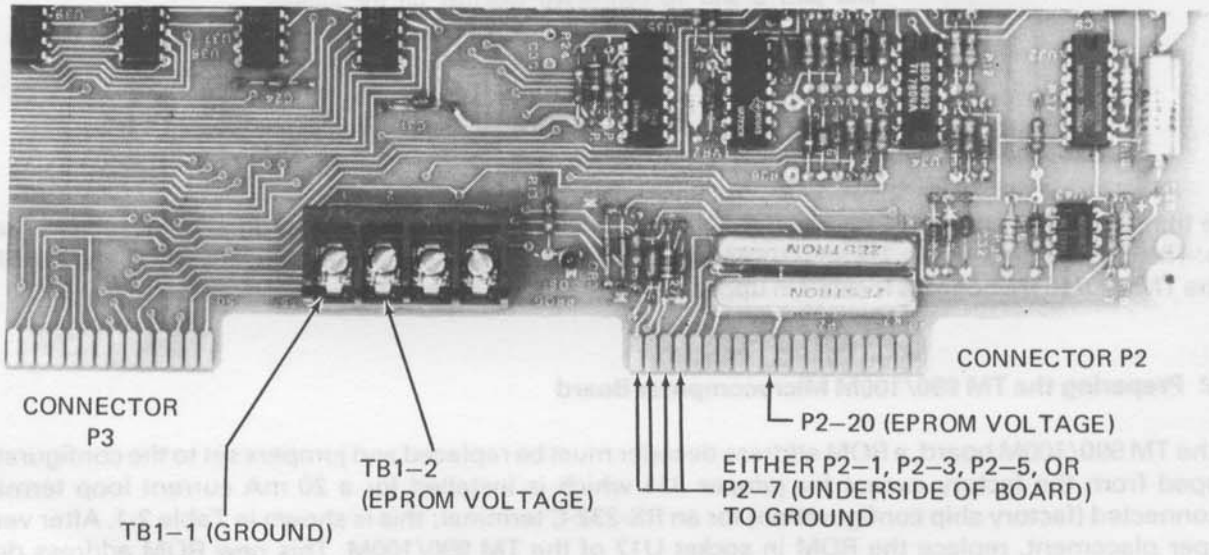
2.5.1 Memory Mapping Change on Microcomputer Boards

The TM 990/302 Software Development Board software does not utilize the standard memory addressing on the TM 990/10X microcomputer boards. On these boards, standard memory configuration has random access memory (RAM) located in the highest memory addresses while eraseable read-only memory (EPROM) begins at addresses 0000_{16}. The SDB software requires an opposite configuration with RAM in lower memory and the EPROM on the microcomputer board disabled. The SDB system software will be resident in upper memory on the TM 990/302 board. Figure 2-2 depicts the memory map of the TM 990/302 operating system using both boards. It is assumed that:

- Both microcomputer boards are fully populated with RAM.
- Onboard RAM on the TM 990/100M is mapped from M. A. 0000_{16} to $03FF_{16}$.
- Onboard RAM on the TM 990/101M is mapped from M. A. 0000_{16} to $0FFF_{16}$.



a) Power Connections to TM 990/510/520 Card Cage from TM 990/518 Power Supply

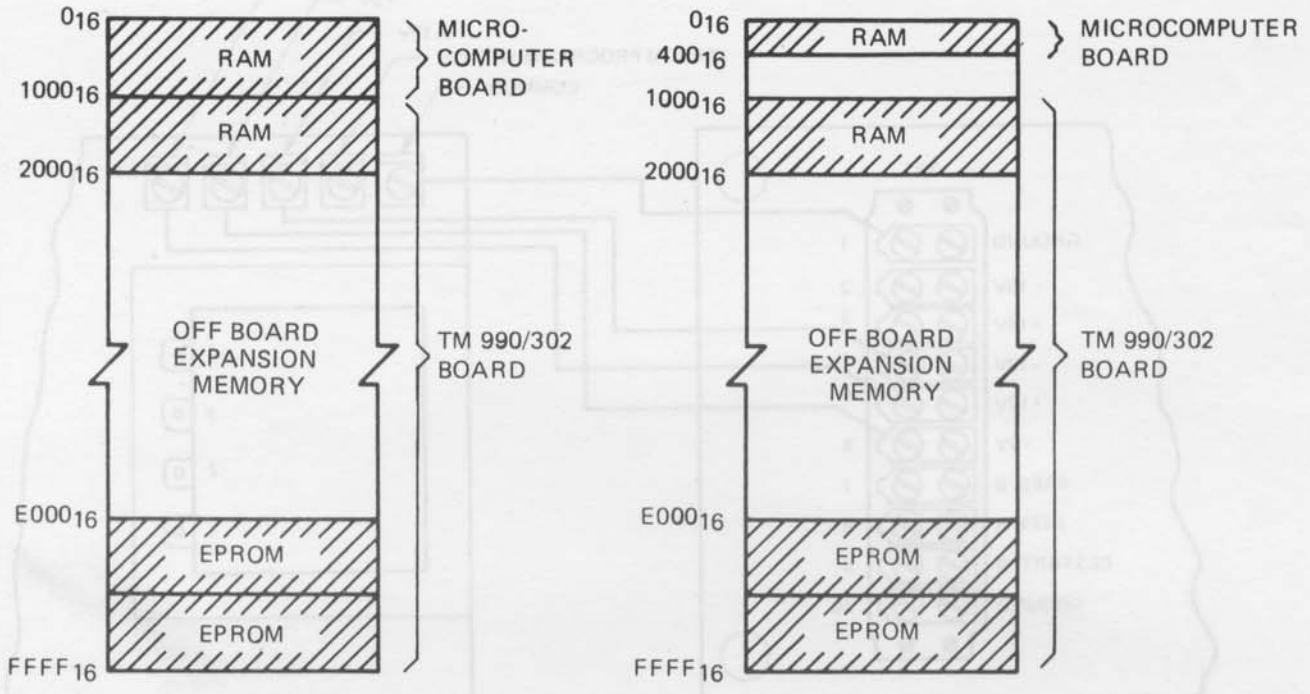


b) EPROM Programming Power Connections to Terminal TB1 of TM 990/302 Board

c) EPROM Programming Power Connections to Connector P2 of TM 990/302 Board

NOTE: User can choose which method of attaching EPROM programming voltage (b or c) is preferred.

Figure 2-1. Power Connections to Software Development System



a) Using TM 990/101M Microcomputer

b) Using TM 990/100M Microcomputer

NOTE: Configuration is shown with switch S1 set to all ones and pins 9 and 10 connected together on the jumper sockets of the TM 990/302 board. Memory mapping of the TM 990/302 board is explained in paragraph 2.9.

Figure 2-2. Memory Configuration for the Software Development System

Note that the entire onboard EPROM area of both microprocessors is eliminated from the system memory map: The EPROM area on the TM 990/100M board is disabled by a new address decode ROM, and the EPROM on the TM 990/101M board is located in upper memory but not accessed by the system.

2.5.2 Preparing the TM 990/100M Microcomputer Board

On the TM 990/100M board, a ROM address decoder must be replaced and jumpers set to the configuration as shipped from the factory except for jumper J11 which is installed for a 20 mA current loop terminal or disconnected (factory ship configuration) for an RS-232-C terminal; this is shown in Table 2-1. After verifying jumper placement, replace the ROM in socket U17 of the TM 990/100M. This new ROM address decoder changes the addressing scheme so that the microcomputer RAM is in lower memory and microcomputer EPROM is disabled. The new decode ROM is shipped on the TM 990/302 board, installed in socket XU12. ROM placements are shown in Figure 2-3. Replace the ROM as follows:

- Remove the replacement ROM from socket XU12 on the TM 990/302 board, and remove the ROM supplied with the TM 990/100M in socket U17; temporarily place the latter ROM in a convenient location. Note that the new ROM replacement is marked "2212017 U12" and the ROM to be replaced is marked "991575 U17".

- Position the replacement ROM in socket U17 of the 990/100M (as indicated by the U number marked on the ROM). Positioning of ROM pin 1 is as shown in Figure 2-3.

- Carefully press the replacement ROM into the socket on the TM 990/100M board until the ROM is firmly seated. Visually verify that pins are not bent and that they make correct contact.

- Place the old ROM in the socket on the TM 990/302 board that held the replacement ROM (which is now in the TM 990/100M board).

TABLE 2-1. JUMPER CONNECTIONS ON THE TM 990/100M BOARD

Jumper	Purpose	Set to Position*
J1	TMS 9901 interrupt	P1-18**
J2, J3, J4	EPROM type	DC
J5, J6, J8	Multidrop interface	DC
J9, J10, J12		
J7	EIA/Multidrop select	EIA
J11	EIA/20mA current loop select	Install for 20 mA, Disconnect for EIA**
C5	RESTART	Not installed**

*DC = Don't care; no change required for use in TM 990/302 configuration
**Position as shipped at factory

2.5.3 Preparing the TM 990/101M Microcomputer Board

On the TM 990/101M board, a new decode ROM is not necessary because the memory decode changes (RAM in lower memory, onboard EPROM disabled) are caused by jumper changes (Table 2-2). On the TM 990/101M, insert jumper E12-E13 to disable onboard EPROM (TIBUG is not used), and insert jumper E15-E16 to reposition RAM/EPROM addressing so that RAM is in lower memory and EPROM is in upper memory. If a teletypewriter is attached to port P2, insert a jumper at E36-E37. All other jumpers are as installed at the factory, indicated in Table 2-2.

2.5.4 Install the Microcomputer Board into the Card Cage

Verify that power is *not* applied to the card cage. Install the microcomputer board into the chassis.

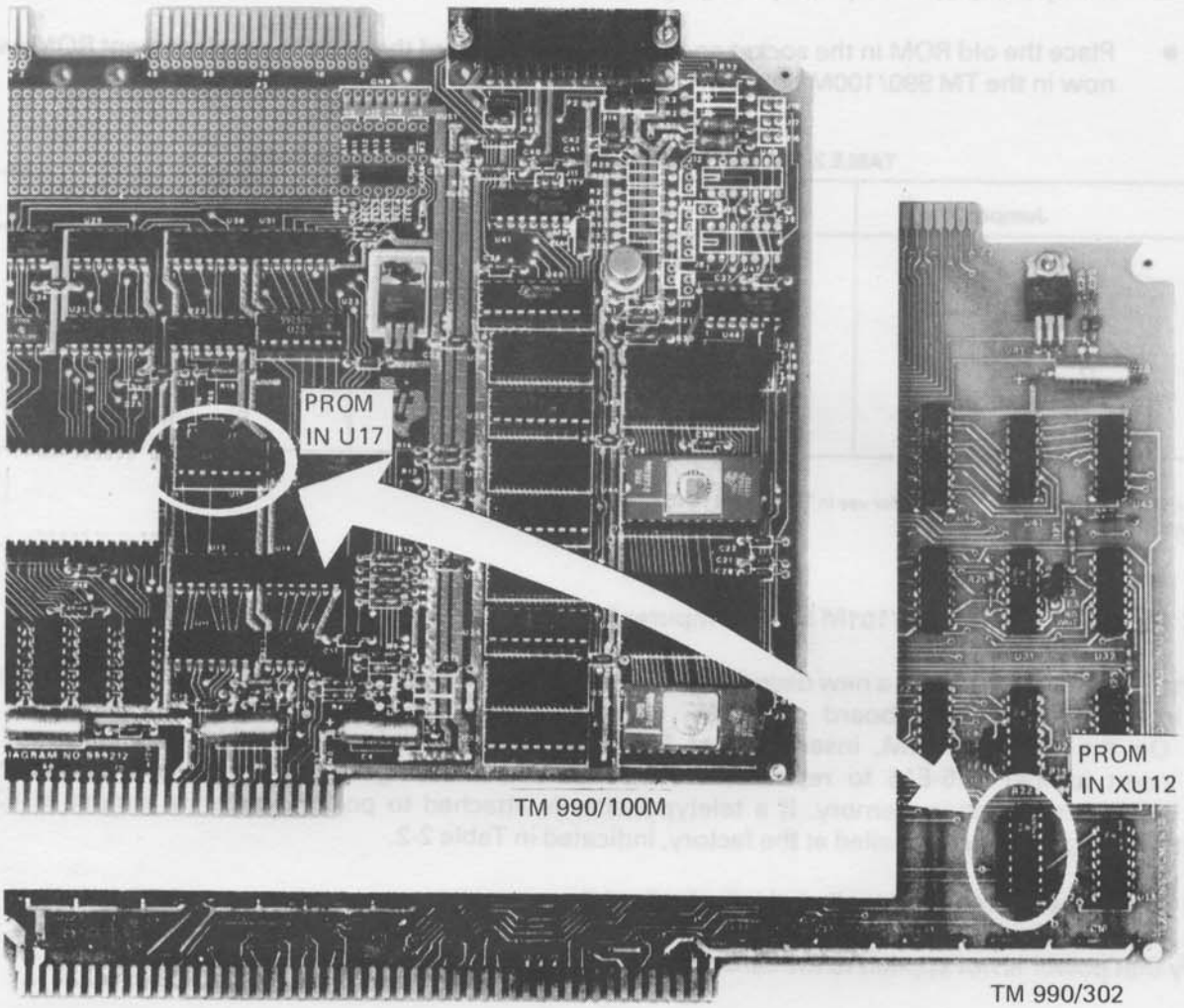
2.6 SET UP AND INSTALL TM 990/302 BOARD

Memory mapping of the TM 990/302 board can be changed by settings of S1 (a four position DIP switch), two jumpers, and a solderable jumper platform on the TM 990/302 board. Changing the TM 990/302 memory map is explained in paragraph 2.9. For applications as shipped from the factory, the memory mapping will be for EPROM on the TM 990/302 containing system software, with a memory map as shown in Figure 2-2. For this configuration, switch S1 and the two jumpers should be as shipped from the factory:

- Switch S1: all four switches set to ON

- Jumper sockets: E1 to E2 and E4 to E5.

With settings as desired, install the TM 990/302 board into the card cage.



PROM EXCHANGE PROCEDURE:

1. Remove PROM in socket U17 on TM 990/100M microcomputer board.
2. Remove PROM in socket XU12 of TM 990/302 board and insert it into socket U17 of TM 990/100M board.
3. Insert PROM removed from U17 of TM 990/100M board into socket XU12 of TM 990/302 board for safekeeping.

Figure 2-3. Address ROM Changeout at TM 990/100M Board

TABLE 2-2. JUMPER CONNECTIONS ON THE TM 990/101M BOARD

Jumper	Purpose	Set to Position*
E1-E2/E2-E3	INT4 from TMS 9902 (local)	E1-E2
E4-E5/E5-E6	INT5 from TMS 9902 (remote)	E4-E5
E7-E8/E8-E53	Wait state for onboard EPROM	DC
E9-E10/E10-E11	TMS 2708/TMS 2716 memory mapping	DC
E12-E13**/E13×E14	Enable/disable onboard EPROM	E12-E13
E15-E16**/E16-E17	RAM/EPROM mapping	E15-E16
E18-E19	Pin 1 of P3 connected to ground	DC
E20-E21	Microterminal power +5 V	DC
E22-E23	Microterminal power +12 V	DC
E24-E25	Microterminal power −12 V	DC
E27-E28/E29-E30	EPROM is TMS 2708	DC
E26-E27/E28-E29	EPROM is TMS 2716	DC
E32-E33/E34-E35	Expansion EPROM is TMS 2708	DC
E31-E32/E33-E34	Expansion EPROM is TMS 2716	DC
E36-E37	Teletype terminal at P2	(E36-E37 if TTY required)
E38-E39	Multidrop at local port	DC
E39-E40	EIA or TTY at P2	E39-E40**
E54-E55	Port P3 EIA compatible	E54-E55**
E55-E56	Port P3 modem compatible	Not Installed
C25	RESTART	Not installed**

*DC = Don't care; no changes required for use in TM 990/302 configuration
**Position as shipped at factory

2.7 AUDIO CASSETTE OPERATION

2.7.1 Connect the Tape Recorders to the TM 990/302

Although the system can be operated with one recorder, a system operates optimally with two tape recorders. Connect the tape recorders as follows:

(1) Tape recorders operate in either a playback or record mode. The TM 990/508 cable joins the TM 990/302 board (connector P2, right side viewed from card cage front) to one or two recorders. At the recorder(s), attach the four labeled leads of the TM 990/508 cable (T1 to T4) and attach a dummy plug as follows:

a. At the playback cassette unit, attach leads of cable TM 990/508 as follows:

- Lead marked "RD MOTOR" to the motor control jack (REMOTE) of the playback unit.
- Lead marked "RD DATA" to the earphone output jack (EAR or MONITOR) of the playback unit.

b. At the record cassette unit, attach leads of cable TM 990/508 as follows:

- Lead marked "WR DATA" to the auxiliary (AUX) input jack of the record unit.
- Lead marked "WR MOTOR" to the write motor control jack (REMOTE) of the record unit.

CAUTION

Do not insert a plug into the MIC socket.

NOTE

A schematic of the TM 990/508 cable is provided in Appendix C.

(2) Attach the female connector of the TM 990/508 cable to edge connector P2 on the right side (facing) of the TM 990/302.

CAUTION

Do not operate the tape recorders on battery power as this could cause varying motor speeds in recording and playback.

During playback do not adjust volume or tone. These must be preset and left. Scratchy volume and tone controls can cause fallout of data. For proper settings see (5).

(3) Install tape cassettes into the recorder/players.

(4) Turn on the tape recorder/players.

(5) Set the tape machine volume control to between 70 percent and 90 percent fully on, and the tone control set to 80 to 100 percent toward treble.

2.7.2 Recorder/Player Protocal

The SDB software does not perform tape rewind operation; thus the user is responsible for rewinding the tape before a read or write operation, and also for loading the tape to the area of magnetic oxide before a write.

Before writing on the tapes, the tapes must be rewound to the clear leader, then brought forward over the magnetic oxide area, erasing the magnetic oxide area of any possible header coding from previous write operations. The write operation begins with writing the header for the to-be-recorded data.

In a read operation, the software looks for a header which is an area of tape containing code identifying the start of data. Data following the header code is considered to be recorded data. Reading of clear leader and unformatted signals on unrecorded tape will not interfere with finding the header area.

2.7.3 Motor Control Plugs and Recorder Motor Control Keys

Before any of the motor control keys on the recorder/player can be used, the lead plugged into the motor control socket at the recorder/player must be removed.

If the next function to the tape is a write:

- remove the plug (if inserted)
- position the tape head over the magnetic oxide of the tape
- insert the plug
- press the RECORD key on the recorder/player.

If the next function to the tape is a read:

- remove the plug (if inserted)
- position the tape head at clear leader or the beginning of data
- insert the plug
- press the PLAYBACK key on the recorder/player.

2.7.4 Cassette Recorder/Player Checkout

The tape recorder that is being used can be checked out for the following:

- Correct head alignment
- Speed variations
- Sound fade
- Poor frequency response (treble or bass response)
- Crosstalk

Head alignment may be checked by producing a test tape on the recorder being evaluated and playing back the test tape on another recorder. If the playback is satisfactory, the recorder that is being evaluated is performing satisfactorily.

Speed variations, sound fade, and poor frequency response can be detected by carefully listening to a known good tape. Recorder speed variations seem to show up best when the test tape is recorded on the recorder under evaluation and played back on a known good recorder.

Crosstalk can be checked using the following procedure:

(1) Erase both sides of the tape
(2) Record on side 1 only
(3) Rewind and listen to side 2
(4) Side 2 should be relatively noise free.

2.8 ATTACH TERMINAL

Attach a terminal to connector P2 of the microcomputer board as shown in Figure 2-4. Cables are listed in Table 2-3.

TABLE 2-3. TERMINAL-MICROCOMPUTER CABLES

Cable Number	Connects
TM 990/501	Connector kit for custom wiring
TM 990/502	RS-232-C terminal
TM 990/503	Texas Instruments 743/745 terminal
TM 990/504	Model 33 ASR teletypewriter modified for 20 mA current loop
TM 990/505	Texas Instruments 733 ASR terminal

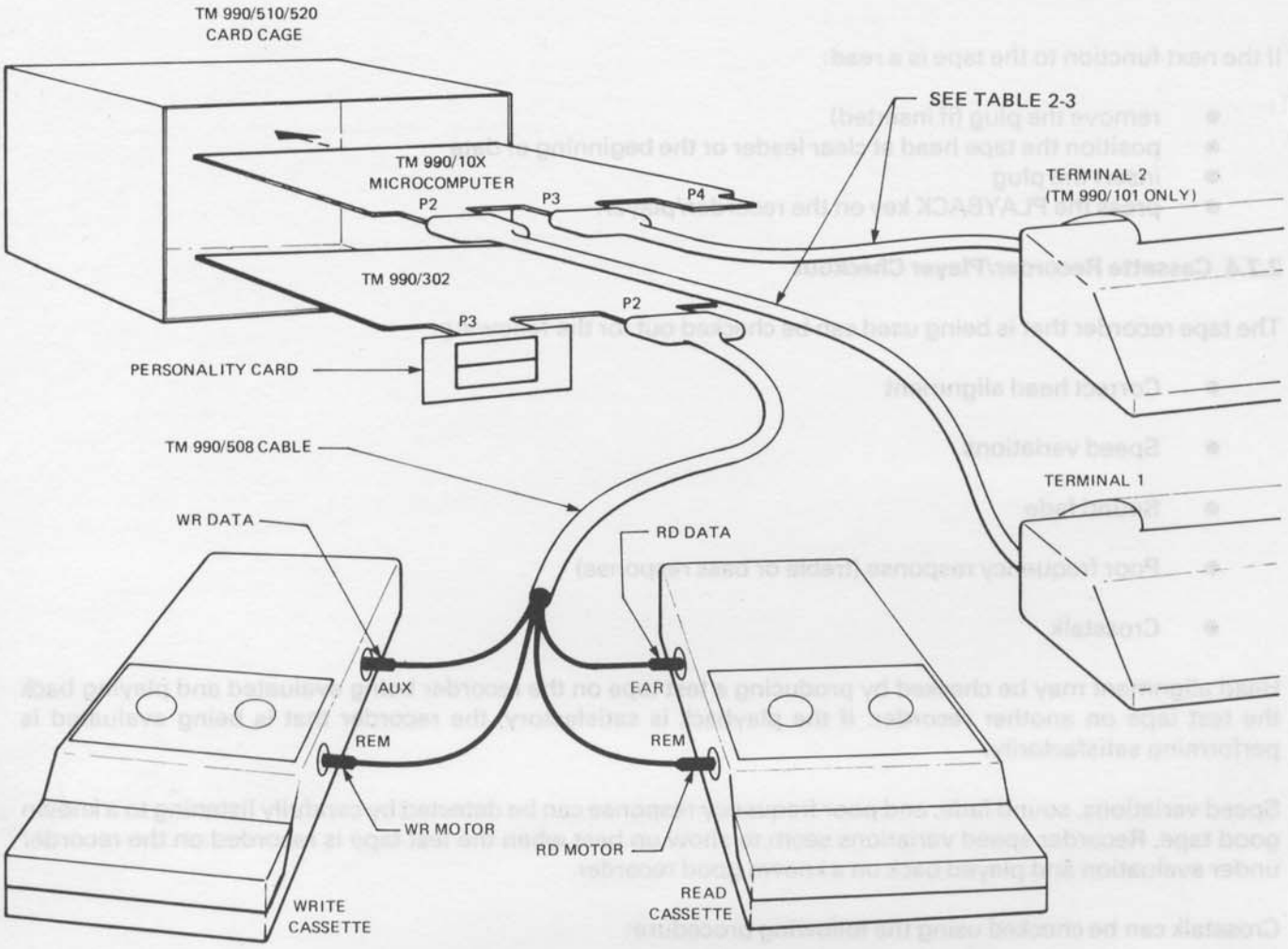


Figure 2-4. Cabling Between Boards and Peripherals

2.9 CUSTOM SYSTEM CONFIGURATION

Configuring the TM 990/302 onboard memory basically requires the setting of DIP switch S1, wiring of jumper platform U25, and the setting of the two jumpers (these are shown in Figure 1-1). Memory mapping of the TM 990/302 board can be custom configured using the following basic steps:

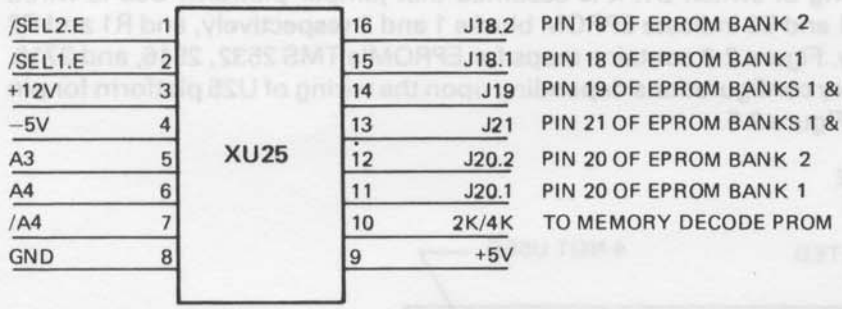
(1) Determine the EPROM type to be used (EPROM's that can be configured in this system include the TMS 2508, TMS 2516, TMS 2716, or TMS 2532). Each memory type requires a specific wiring of the U25 platform. When correctly wired, the specific memory configuration can be selected by a setting of switch S1. Paragraph 2.9.1 describes selection of the desired memory map.

(2) The memory access time should be checked for selection of memory wait states. If devices are utilized that meet the access time requirements, no wait state is needed. As shipped, jumper terminals E1 and E2 should be jumpered for a WAIT state. Paragraph 2.9.2 describes wait states and memory access requirements for various processor speeds and memory types.

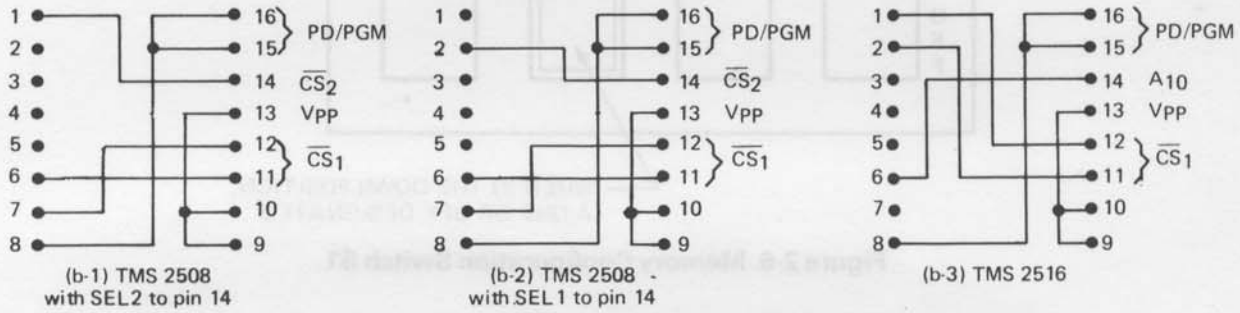
(3) The load circuitry must be enabled if EPROM is in upper memory; thus a jumper between E5 and either E4 (LOAD) or E6 (NO LOAD) is necessary. A description of load logic is found in paragraph 2.9.3.

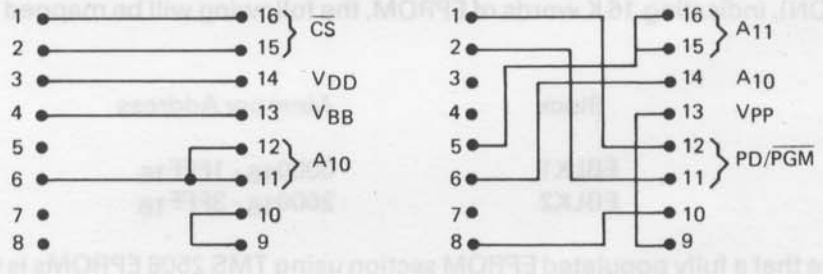
2.9.1 Memory Mapping

The user can employ one of four types of EPROM's on the TM 990/302 board: TMS 2508, TMS 2516, TMS 2716, or TMS 2532. Each EPROM requires a unique wiring of jumper platform U25; these platform schematics are shown in Figure 2-5. Note that EPROM 2508 can use one of two different jumper configurations; this allows it additional memory address configurations.



(a) Socket Schematic





(b) Platform Wiring for Different EPROM Types
(EPROM pin nomenclature on right)

Figure 2-5. Wiring of Platform U25 for Different EPROM Types

Memory mapping is selected according to the setting of switch S1. Only switches 1, 2, and 3 are used; switch 4 is not wired. Figure 2-6 shows how to set switch S1 for custom applications.

Onboard memory is divided into two blocks each of EPROM and RAM as shown in Figure 2-7. This figure identifies the physical location of the memory elements and the resulting socket locations of the most- and least-significant bits.

Available memory map configurations, according EPROM type, switch S1 and jumper platform U25, are shown in Figures 2-8 and 2-9. Each vertical column in the right side of each figure shows a system memory map, and the column heading is a setting of switch S1. It is assumed that jumper platform U25 is wired accordingly for the EPROM type used. E1 and E2 indicate EPROM blocks 1 and 2 respectively, and R1 and R2 indicate RAM blocks 1 and 2 respectively. Figure 2-8 contains maps for EPROM's TMS 2532, 2516, and 2716. Figure 2-9 contains two TMS 2508 memory configurations depending upon the wiring of U25 platform for pin 14 to pin 1 or pin 14 to pin 2 as shown in Figure 2-5.

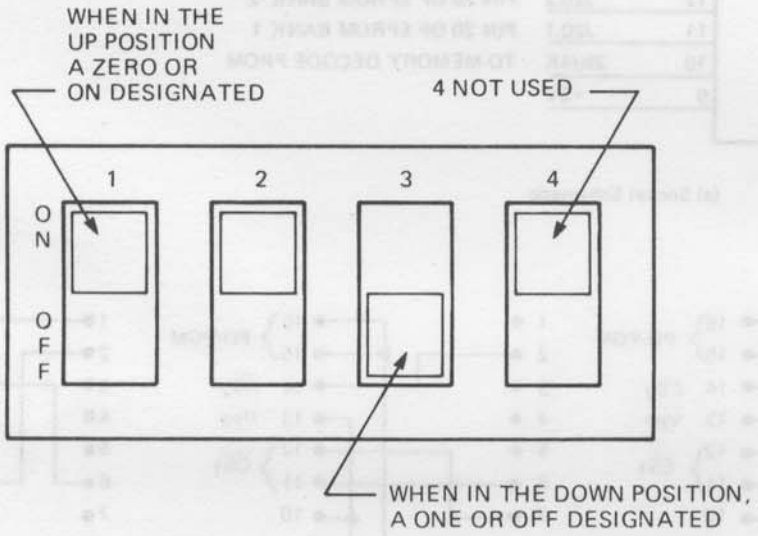


Figure 2-6. Memory Configuration Switch S1

Example 1. Assume that a fully populated EPROM section using TMS 2532 EPROMs is to be used. The jumper platform will be wired as indicated in Figure 2-5 (b-5). If the memory configuration switch (S1) is set to switch code 3 (OFF, OFF, ON), indicating 16 K words of EPROM, the following will be mapped by the memory decode logic:

Block	Memory Address
EBLK1	0000_{16} - $1FFF_{16}$
EBLK2	2000_{16} - $3FFF_{16}$

Example 2. Assume that a fully populated EPROM section using TMS 2508 EPROMs is to be used. The adaptor platform will be wired as indicated in Figure 2-5 (b-1). If the memory configuration switch (S1) is set to switch code 2 (ON, OFF, ON), indicating 4 K words of EPROM, the following will be mapped by the memory decode logic:

Block	Memory Address
EBLK1	0000_{16} - $07FF_{16}$
EBLK2	0800_{16} - $0FFF_{16}$

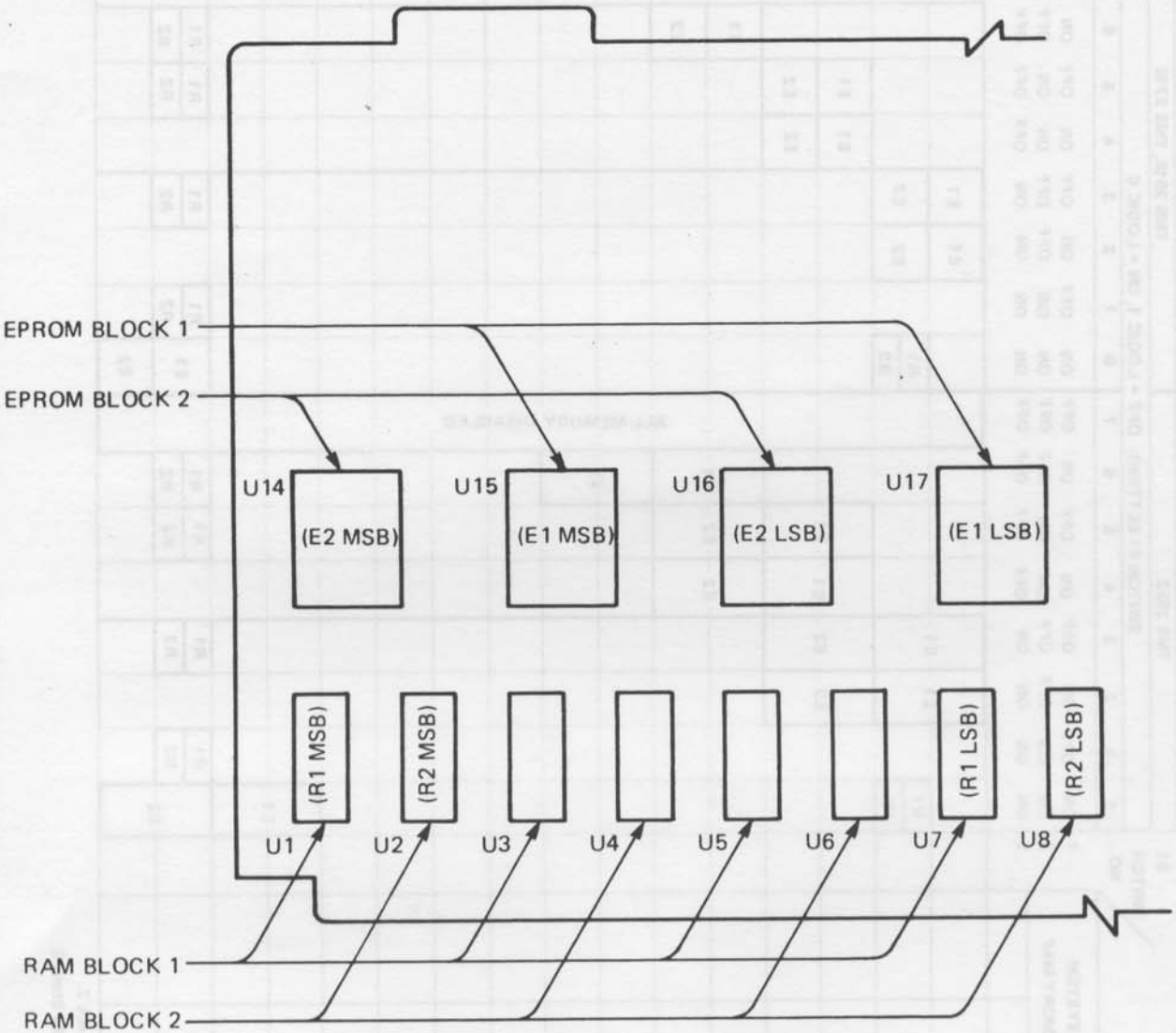
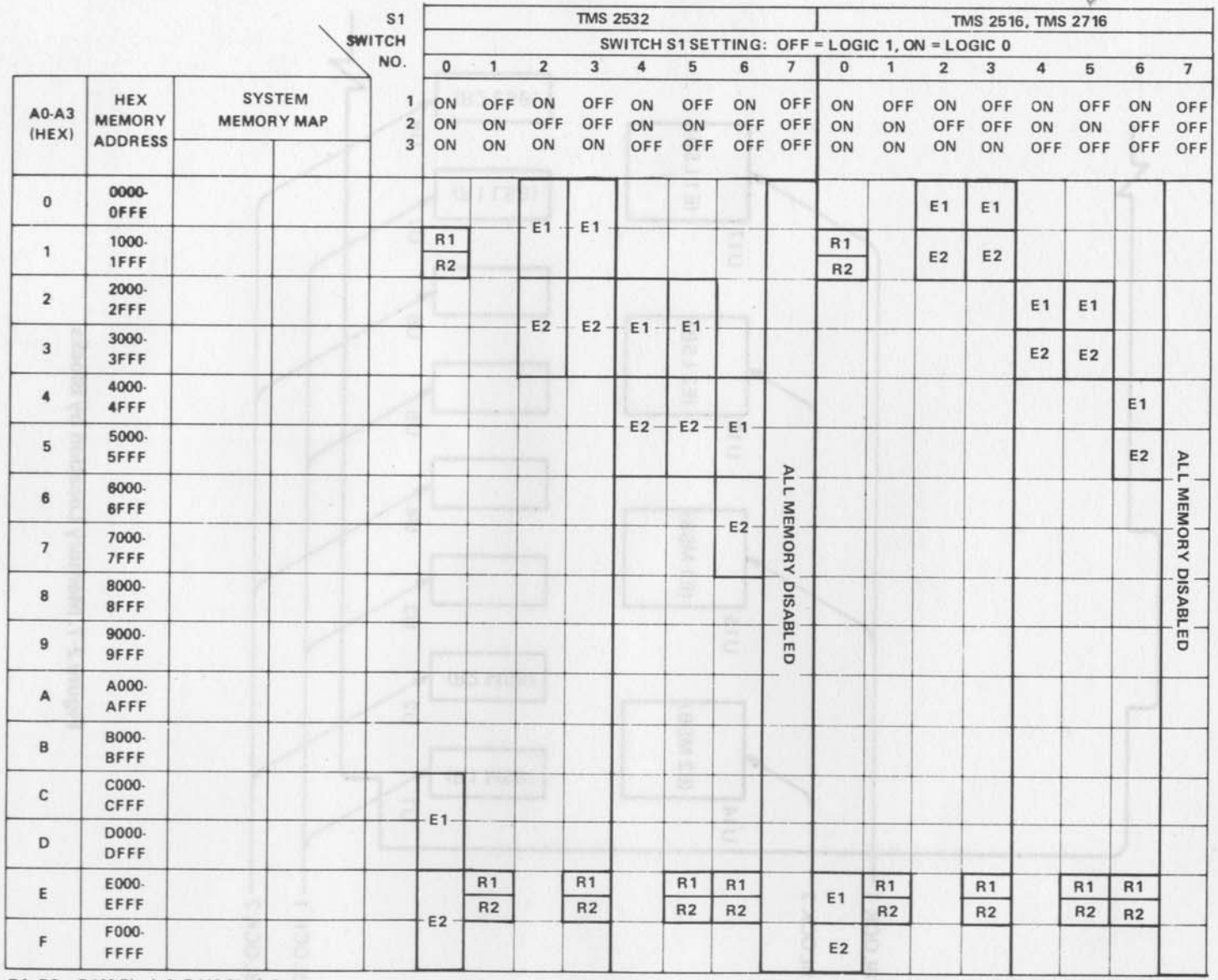
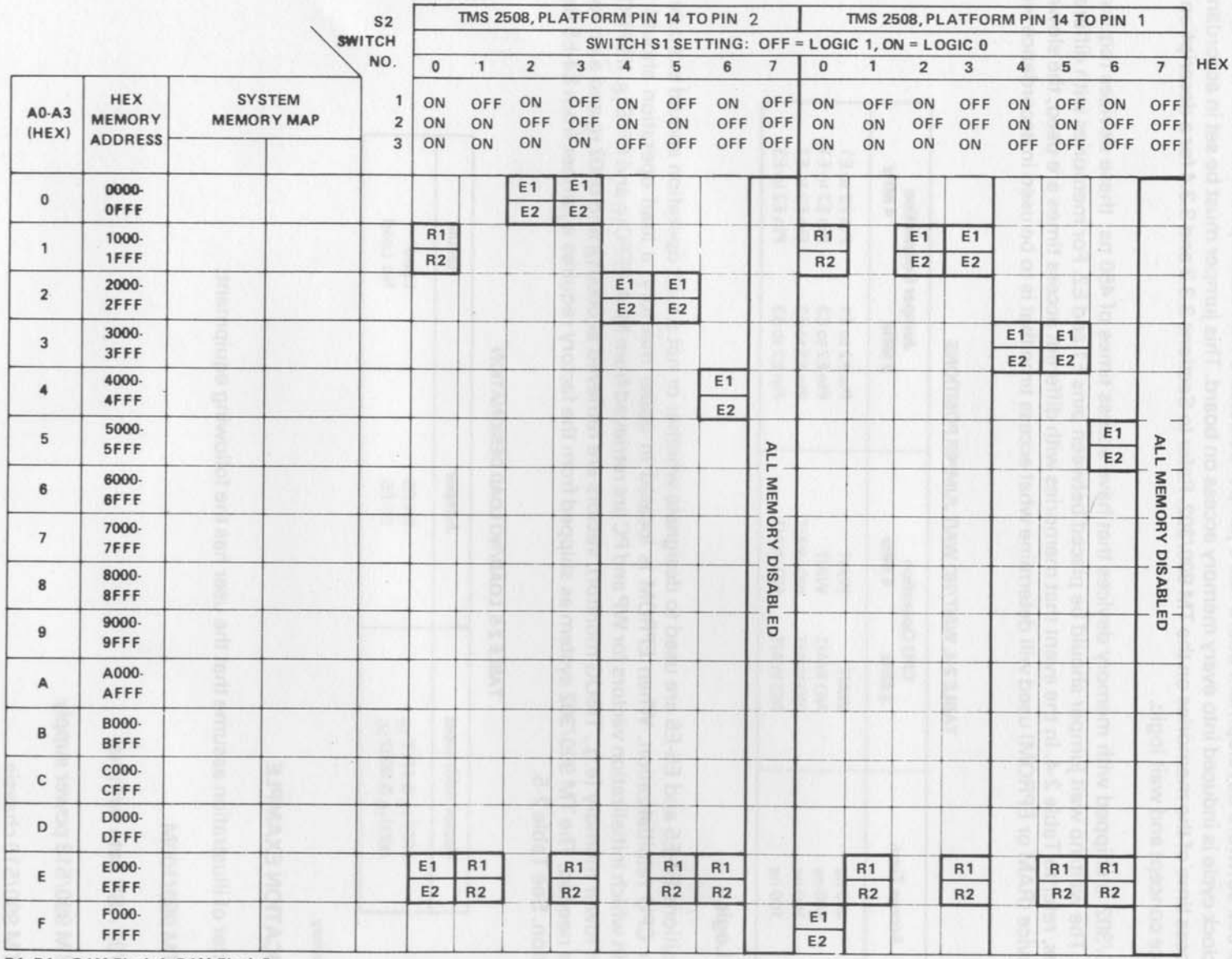


Figure 2-7. Memory Location by Blocks



R1, R2 = RAM Block 1, RAM Block 2
E1, E2 = EPROM Block 1, EPROM Block 2

Figure 2-8. Memory Map for TMS 2516, TMS 2532, and TMS 2716 EPROMs



R1, R1 = RAM Block 1, RAM Block 2
E1, E2 = EPROM Block 1, EPROM Block 2

Figure 2-9. Memory Map for TMS 2508 EPROM

2.9.2 Select Wait State

The TM 990/302 software development board has a jumper selectable wait state option. In 'wait' mode, one additional clock cycle is induced into every memory access on board. This jumper must be set in accordance with the access time of the memories on the TM 990/302. Refer to Sections 3.3.3 and 3.3.4 for a description of the wait state concept and wait logic.

The TM 990/302 is shipped with memory devices that have access times of 450 ns: these devices require a 'wait' state. The wait/no wait jumper should be placed between pins E1 and E2. For memories with different access times, refer to Table 2-4. In the event that memories with different access times are used, the slowest memory device (RAM or EPROM) used will determine what access time that is to be used in accordance with Table 2-4.

TABLE 2-4. WAIT/NO WAIT JUMPER POSITIONS

Access Time	CPU Operation		Jumper Connection	
	3 MHz	4 MHz	3 MHz	4 MHz
450 ns	WAIT	WAIT	Pin E2 to E1	Pin E2 to E1
300 ns	NO WAIT	WAIT	Pin E2 to E3	Pin E2 to E1
200 ns	NO WAIT	NO WAIT	Pin E2 to E3	Pin E2 to E3
100 ns	NO WAIT	NO WAIT	Pin E2 to E3	Pin E2 to E3

2.9.3 Load Logic

Jumper positions E4-E5 and E5-E6 are used to designate whether or not a load operation should execute at powerup or CPU reinitialization. When EPROM is located in upper memory, a load operation should be performed in which initialization vectors for WP and PC are retrieved from M. A. $FFFC_{16}$ and $FFFE_{16}$. If EPROM is located in lower memory (e.g., TIBUG monitor), vectors are retrieved at 0000_{16} and 0002_{16} and a no-load operation is needed. The TM 990/302 system as shipped from the factory requires a jumper from E4-E5 for a load operation. See Table 2-5.

TABLE 2-5. LOAD/NO LOAD DESIGNATION

Vector Addresses	Jumper	Result
$FFFC_{16}$ & $FFFE_{16}$	E4-E5	Load*
0000_{16} & 0002_{16}	E5-E6	No-Load

*Jumpered at factory

2.10 APPLICATION EXAMPLE

For the matter of illustration assume that the user has the following equipment:

- TM 990/100M
- 733 ASR data terminal
- TM 990/518 power supply
- TM 990/510 chassis
- TM 990/302-1 software development board. (With TM 990/514 EPROM personality module and TM 990/302 software development package)

The required memory map is shown in Figure 2-10. This figure shows the TM 990/100M memory map, the TM 990/302 memory map and the required memory map. Note that the EPROM memory on the TM 990/100M is in conflict with the desired overall system memory. The TM 990/302 is supplied with an alternate memory decode PROM U12, that when taken from the TM 990/302 and installed in place of U17 on the TM 990/100M reconfigures the TM 990/100M memory map. The socket for U12 on the TM 990/302 can be used to store the original U17.

This alternate memory decode PROM configures the TM 990/100M's RAM area into location 0_{16} through $3FE_{16}$, the entire EPROM area is disabled and the memory mapped I/O remains unchanged. For more information on TM 990/100M memory decoding refer to TM 990/100M Microcomputer Users Guide.

Because the system EPROM and thus the program resides at high memory, a load must be performed in order to initialize execution at the proper address. In this case the load jumper on the TM 990/302 must be set in the 'LOAD' position. This allows a load pulse to be generated by the TM 990/302 when the reset switch on the TM 990/100M is pushed and released.

The wait jumper should be set to the 'WAIT' position to allow sufficient memory cycle time for the memories supplied on the TM 990/302.

If EPROMs are to be programmed, 35 V to 55 V unregulated is applied to pin 1 and 2 of terminal block TB1. Pin 2 is the most positive terminal and care must be taken not to introduce ground violations. But the use of the TM 990/518 power supply precludes this possibility. The appropriate EPROM programming module can now be placed on P3 (the 50 pin edge connector).

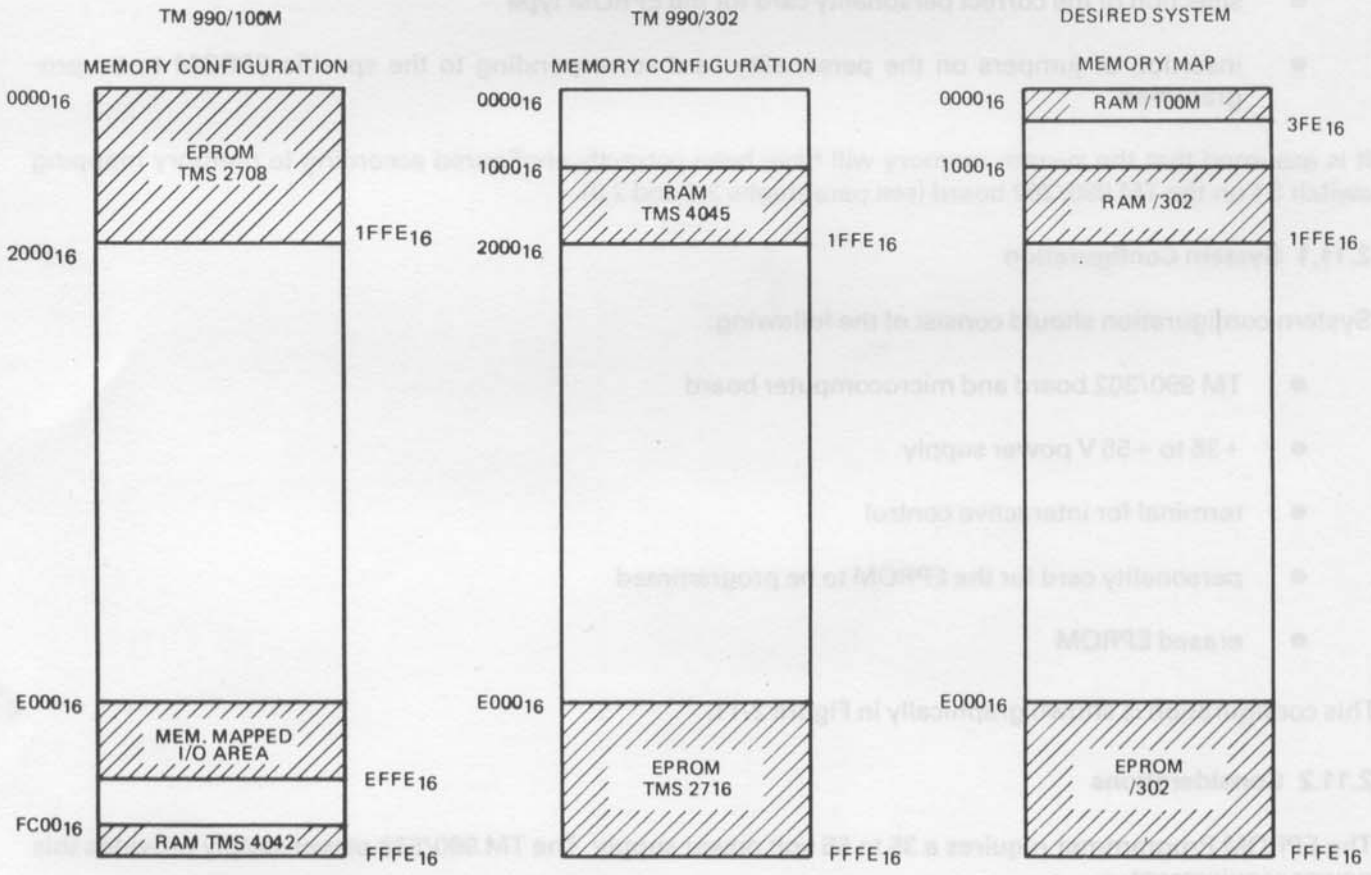


Figure 2-10. Example TM 990/302 System Memory Map

Note that the 'GO' LED is lit when power is supplied. If not, the module has been plugged in upside down and must be turned around.

After terminal and power are properly applied and the boards are seated firmly in the chassis, apply power, reset, and type a carriage return on the terminal. The system is now operational.

2.11 EPROM PROGRAMMER

Using applicable software, the EPROM programmer can program the following EPROMs:

- TMS 2708 EPROM
- TMS 2716 EPROM
- TMS 2508 EPROM
- TMS 2516 EPROM
- TMS 2532 EPROM

Two hardware selections must be made before the erased EPROM can be inserted and the EPROMs programming software called up. These include:

- selection of the correct personality card for the EPROM type
- insertion of jumpers on the personality card corresponding to the specific EPROM to be programmed

It is assumed that the system memory will have been correctly configured according to memory mapping switch S1 on the TM 990/302 board (see paragraphs 2.6 and 2.9).

2.11.1 System Configuration

System configuration should consist of the following:

- TM 990/302 board and microcomputer board
- +35 to +55 V power supply
- terminal for interactive control
- personality card for the EPROM to be programmed
- erased EPROM

This configuration is shown graphically in Figure 2-11.

2.11.2 Considerations

The EPROM Programmer requires a 35 to 55 volt power supply. The TM 990/518 power supply provides this power requirement.

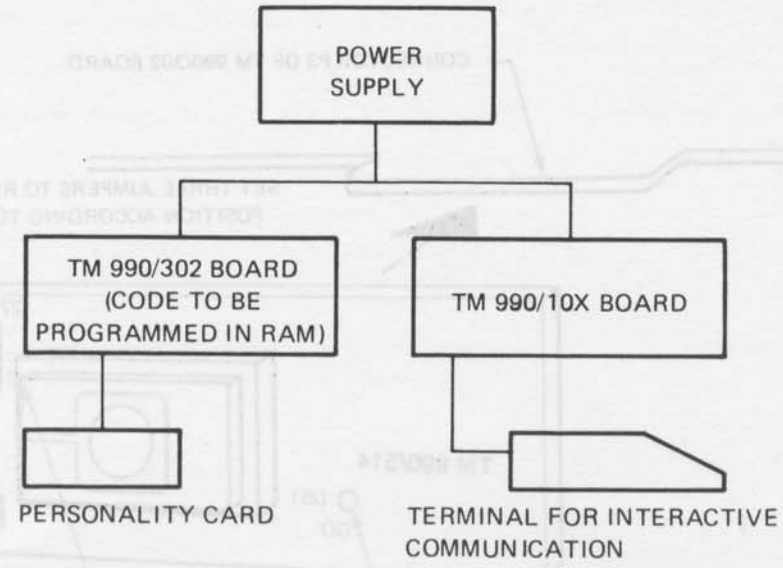


Figure 2-11. Typical EPROM Programming Configuration

2.11.3 EPROM Erasure Procedure

The EPROM can be erased by exposing the chip to ultraviolet light (wavelength of 2537 angstroms) through the transparent window on the chip. Recommended exposure is ten watt-seconds per centimeter which is equivalent to approximately 30 minutes exposure to a filterless model S52 short wave ultraviolet lamp approximately 2.5 centimeters above the EPROM. EPROM erasure state is all ones.

2.11.4 System Setup

2.11.4.1 EPROM Personality Card

An EPROM personality card attaches to the TM 990/302 SDB board at connector P3 as shown in Figure 2-12. This card provides the socket to hold the EPROM as well as interface circuitry between the TM 990/302 and the EPROM.

There are two personality cards available for the TM 990/302. As shown in Table 2-6, each card is used for programming more than one EPROM type.

TABLE 2-6. PERSONALITY CARD CHARACTERISTICS

For Programming	Part Number
TMS 2708 and TMS 2716 TMS 2508, TMS 2516, & TMS 2532	TM 990/514 TM 990/515

To insert the personality card, press the female connector on the back of the personality card on to connector P3 (left side of the TM 990/302 Board). Note the top and bottom of card as shown in Figure 2-12.

2.11.4.2 Insert PROM Into Personality Card, Designate PROM Model

Insert the EPROM to be programmed into the personality card as shown in Figure 2-12. Align the pins with pin one of the EPROM in the top right (facing the card) of the socket on the personality card. Take care to prevent pins from being bent.

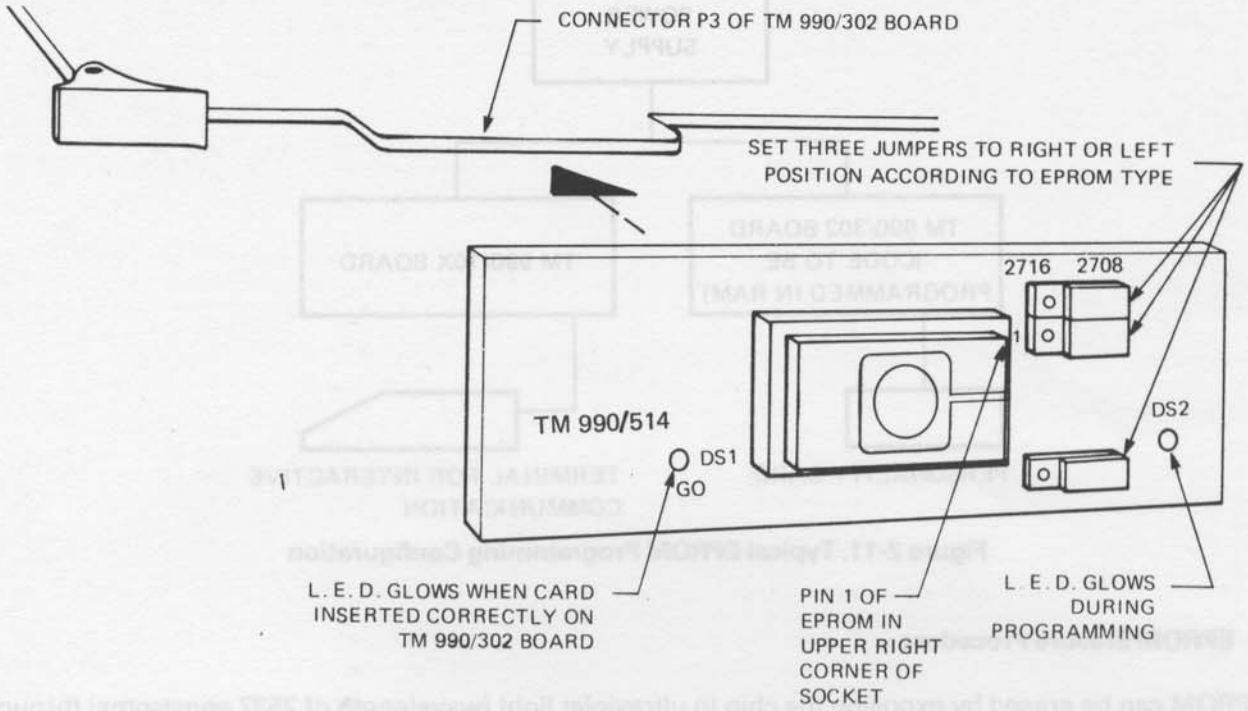


Figure 2-12. Personality Card (TM 990/514)

Two personality cards, as shown in Table 2-6, are used to hold two different EPROM models. To designate which model is being programmed, position the three jumpers on the right side of the card onto the pins corresponding to the PROM model as shown in Table 2-7.

TABLE 2-7. JUMPER PLACEMENT ON PERSONALITY CARD

EPROM Model	Card Number	Jumper Placement on Card
TMS 2708	TM 990/514	2708
TMS 2716	TM 990/514	2716
TMS 2508	TM 990/515	2508
TMS 2516	TM 990/515	2516
TMS 2532	TM 990/515	2532

2.11.4.3 Personality Card L.E.D.s

If the personality card is inserted incorrectly (e.g., upsidedown), the L.E.D. marked GO on the card will be extinguished. When inserted correctly, this light will glow.

The L.E.D. on the right side of the personality card will glow while the EPROM is being programmed.

CAUTION

Do not touch the TM 990/302 board while EPROM voltage is applied. A maximum potential difference of 67 Vdc can exist with the +55 V EPROM voltage applied.

SECTION 3

HARDWARE DESCRIPTION

3.1 GENERAL

An overview of a typical software development setup using the TM 990/302 will be presented first — then the functional block diagram will be introduced and described. The theory involving the three major sections: (1) EPROM and RAM memory, (2) EPROM programmer and CRU interface, and (3) audio cassette interface will be presented next followed by a description of the initialization procedures and load logic.

3.2 SYSTEM OVERVIEW

Figure 3-1 shows a simplified software development system. The major elements of the system are the TM 990/302 software development board, the TM 990/100 microcomputer, TM 990/5XX EPROM personality programming card, TM 990/510 card chassis, a terminal, cassette recorder/recorders, and a power supply such as TM 990/518.

The software program that is to be stored in the EPROM is entered into the system via the terminal in source program format. The source program is edited, assembled and debugged prior to PROM programming the finished software onto the EPROM chip. The cassettes provide an inexpensive method for storing source and object programs.

Figure 3-2 is a block diagram of the TM 990/302 board. The audio cassette interface (ACI) provides relay control for the recorders and waveshaping circuitry for recorder input/output signals. The EPROM and RAM section of the memory contains assembler and monitor programs while providing needed storage space. The EPROM personality card is driven by the EPROM programmer buffer circuitry.

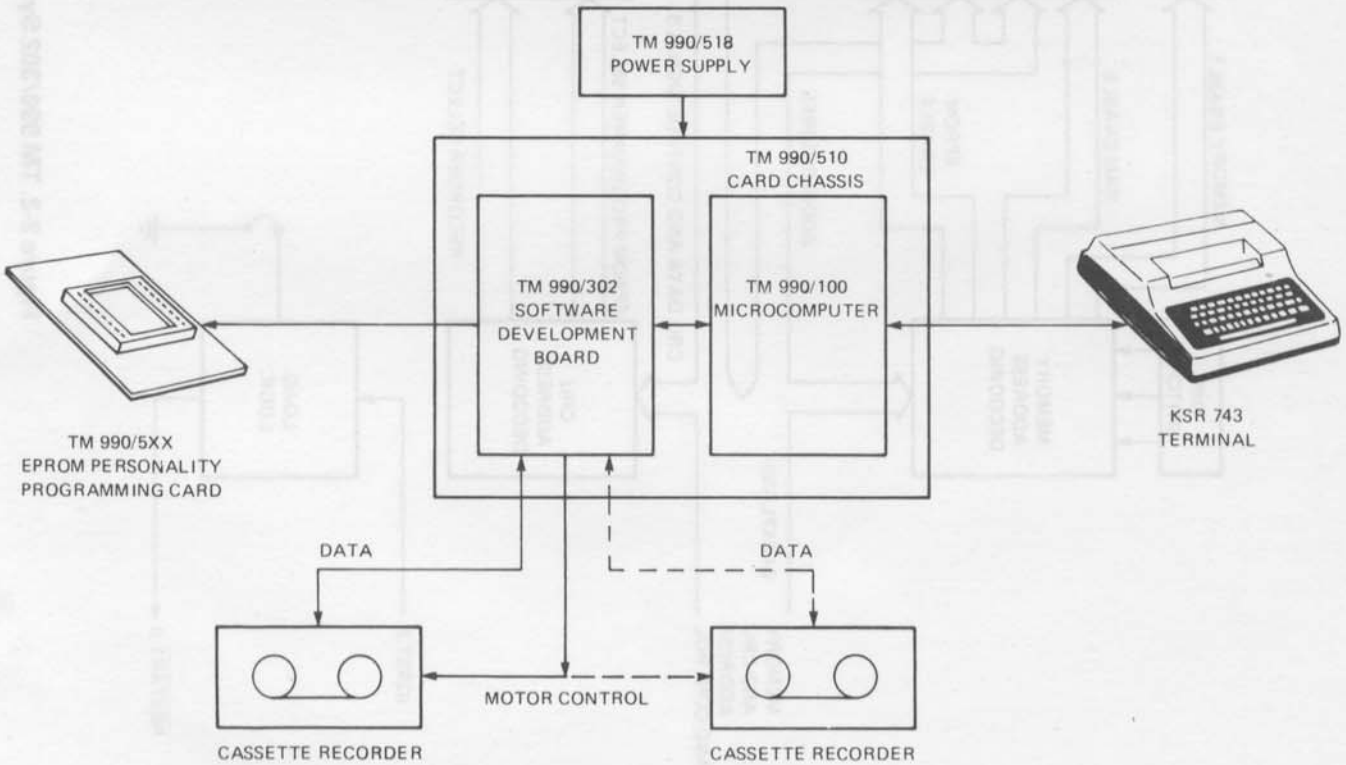


Figure 3-1. Software Development System

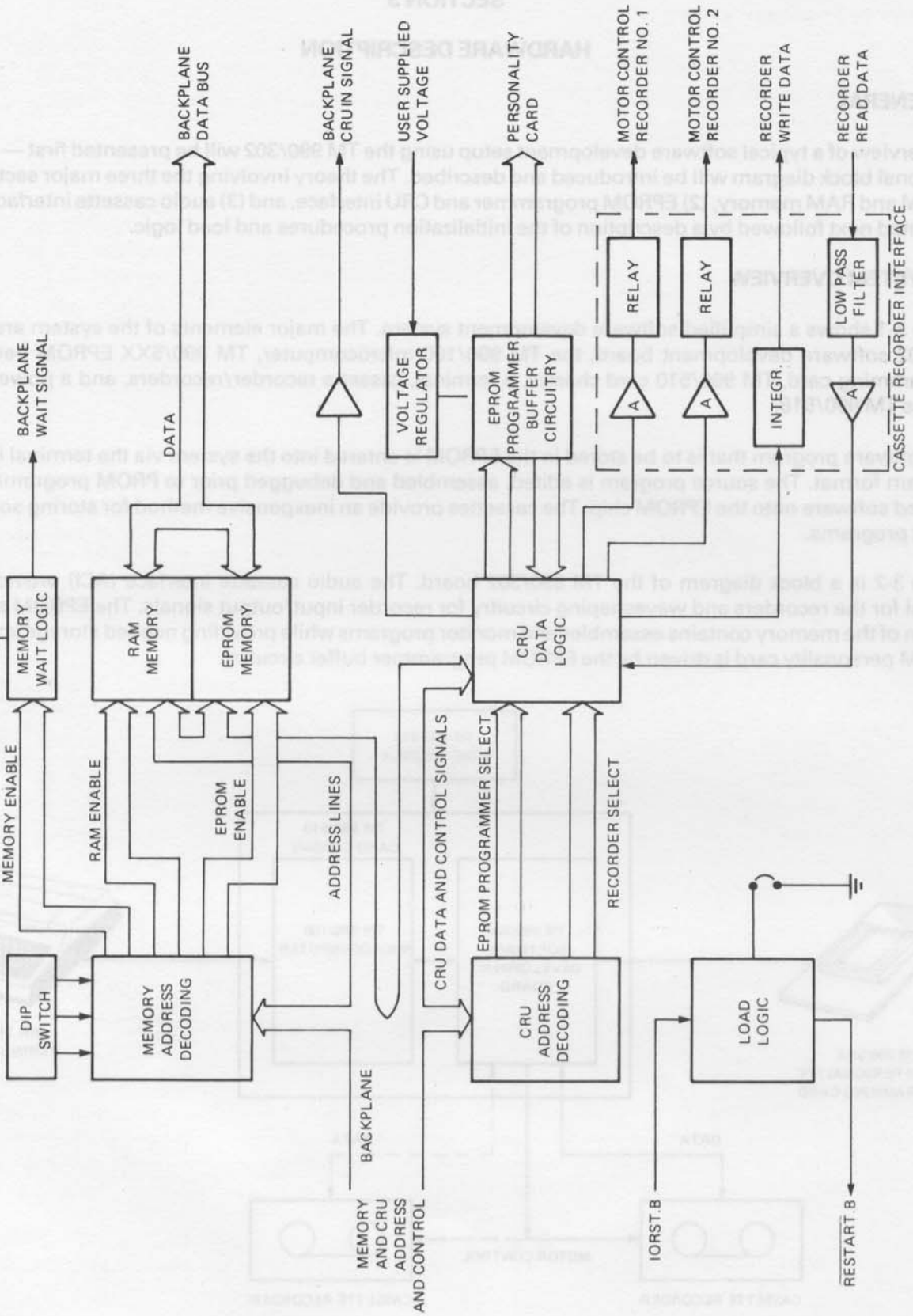


Figure 3-2. TM 990/302 System Functional Block Diagram

3.3 EPROM AND RAM MEMORY

Memory on the TM 990/302 whether it is RAM or EPROM is programmed into contiguous blocks. Block 1 is at the lower addresses of the block and Block 2 occupies the upper addresses of the block. Figure 2-7 shows memory placement by blocks.

3.3.1 RAM Memory

The RAM memory available on the TM 990/302 software development board consists of 2K words of TMS 4045 static RAM (1K by four bits each). This RAM memory can be configured as shown in Figures 3-3 or 3-4 (Figure 3-3 is the standard memory map while Figure 3-4 shows memory broken down into blocks.) These maps are the combined TM 990/302 EPROM and RAM memory maps. Note that signal 2K/4K at jumper platform U25 is +5 V for all EPROM types except the TMS 2532 where it is tied to ground. Refer to section 3.3.5 for a description of the memory decoding logic on the TM 990/302.

3.3.2 EPROM Memory

The EPROM area of the TM 990/302 accomodates a number of different EPROM types. This facilitates testing of software programmed into EPROM by the user. For a description of EPROM decoding and wiring of EPROM configuration platform see section 3.3.5.

The RAM and EPROM on the TM 990/302 board have a very flexible memory map which is almost totally controlled by memory decode PROM U28. If an alternate memory map is required, the user can program an alternate 74S287 for this purpose. For an example of programming an alternate PROM, see Appendix D.

Since the memory devices on the TM 990/302 drive the bus directly, the devices removed from the board release the memory area they occupy. This means that if a particular memory is removed from its socket, then the area in memory where it is mapped is now free for use by another device. This greatly increases the flexibility of the memory space.

NOTES

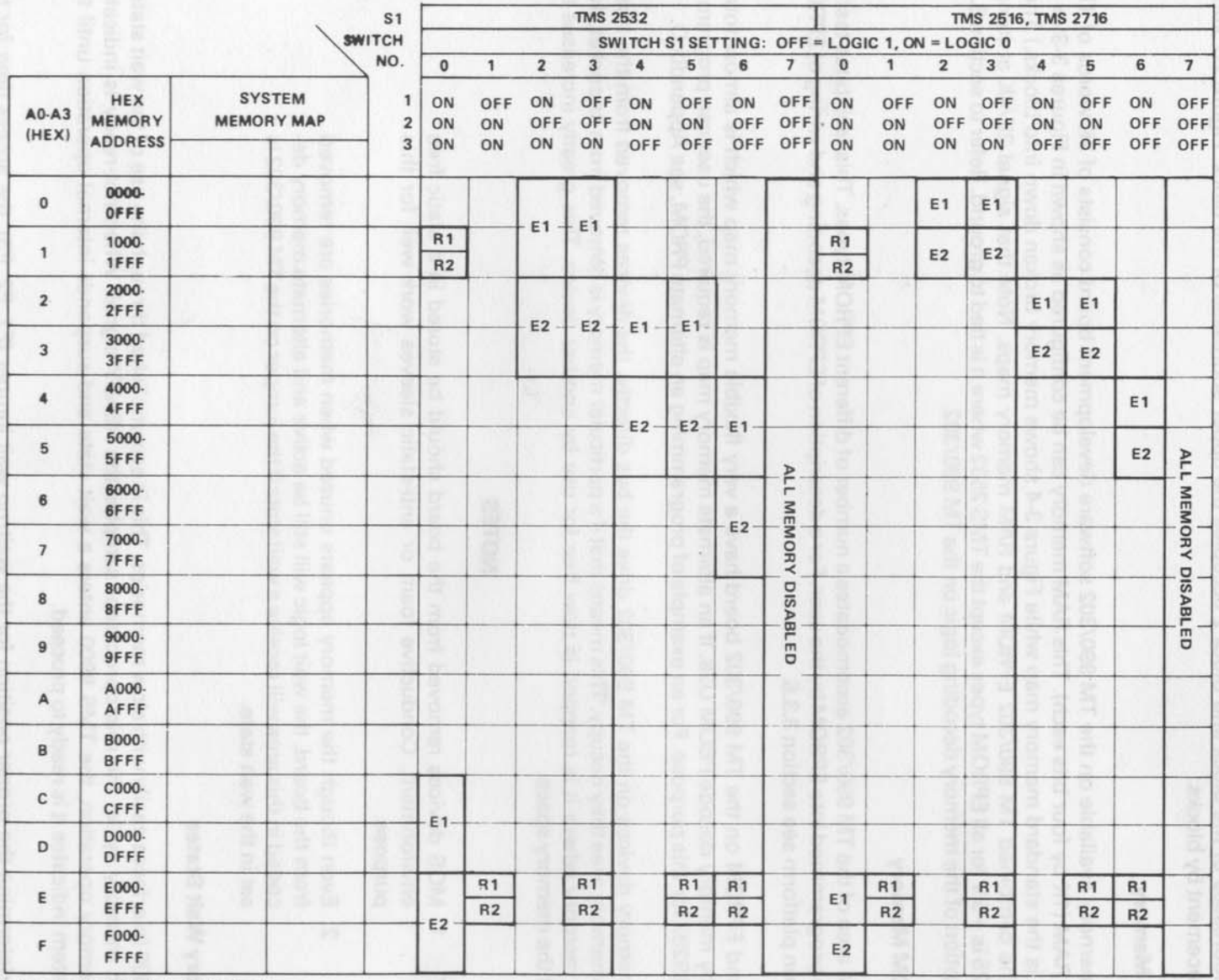
1. MOS devices removed from the board should be stored in a static free environment. Conductive foam or anti-static sleeves work well for this purpose.

2. Even though the memory appears unused when memories are removed from the board, the wait logic will still be active and alternate memory decoded in this area will receive a wait state if the jumper on the TM 990/302 is set in the wait state.

3.3.3 Memory Wait States

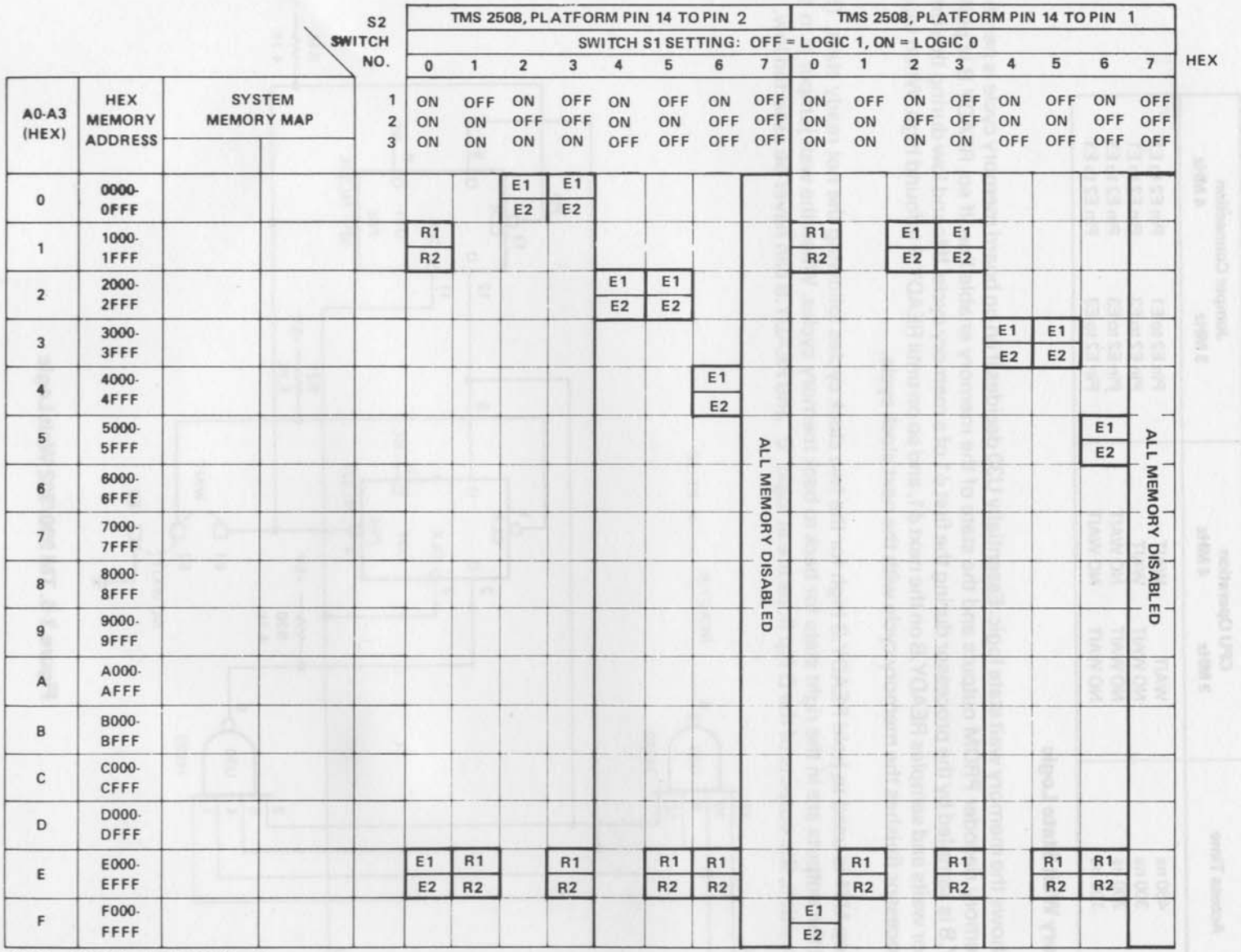
The TMS 9900 interfaces easily with slow memories. This is accomplished through the use of the wait states. During each memory cycle, the microprocessor samples the READY signal. When not-ready is indicated during a memory operation, the TMS 9900 enters a wait state and suspends internal operation until the memory system indicates it is ready to proceed.

In order to determine the proper position for the wait/no wait jumper (E1, E2, E3), the access time for the memory chips and the CPU speed must be known. The proper position for the wait/no wait jumper can be obtained from Table 3-1.



R1, R2 = RAM Block 1, RAM Block 2
E1, E2 = EPROM Block 1, EPROM Block 2

Figure 3-3. Standard Memory Map for TM 990/302



R1, R1 = RAM Block 1, RAM Block 2
E1, E2 = EPROM Block 1, EPROM Block 2

Figure 3-4. Block Memory Map for TM 990/302

TABLE 3-1. WAIT/NO WAIT JUMPER POSITIONS

Access Time	CPU Operation		Jumper Connection	
	3 MHz	4 MHz	3 MHz	4 MHz
450 ns	WAIT	WAIT	Pin E2 to E1	Pin E2 to E1
300 ns	NO WAIT	WAIT	Pin E2 to E3	Pin E2 to E1
200 ns	NO WAIT	NO WAIT	Pin E2 to E3	Pin E2 to E3
100 ns	NO WAIT	NO WAIT	Pin E2 to E3	Pin E2 to E3

3.3.4 Memory Wait State Logic

Figure 3-5 shows the memory wait state logic. Essentially U30 decides if an on board memory cycle is pending from the memory decoder PROM outputs and the state of the memory enable line. If so, READY.B is pulled low. READY.B is sampled by the processor during the first $\phi 1$ of a memory cycle. If found low during this time, the processor waits and samples READY.B on the next $\phi 1$, and so on until READY.B is found high. When found high, the processor finishes the memory cycle with the next clock cycle.

The D flip flop U31 is used to hold READY.B high for the two clock cycles following the not ready state. This insures that the outputs are in the right state for back to back memory cycles. When the wait jumper is in the "no wait" position, the outputs of the D flip flops are at logic "0" and READY.B can never be asserted low.

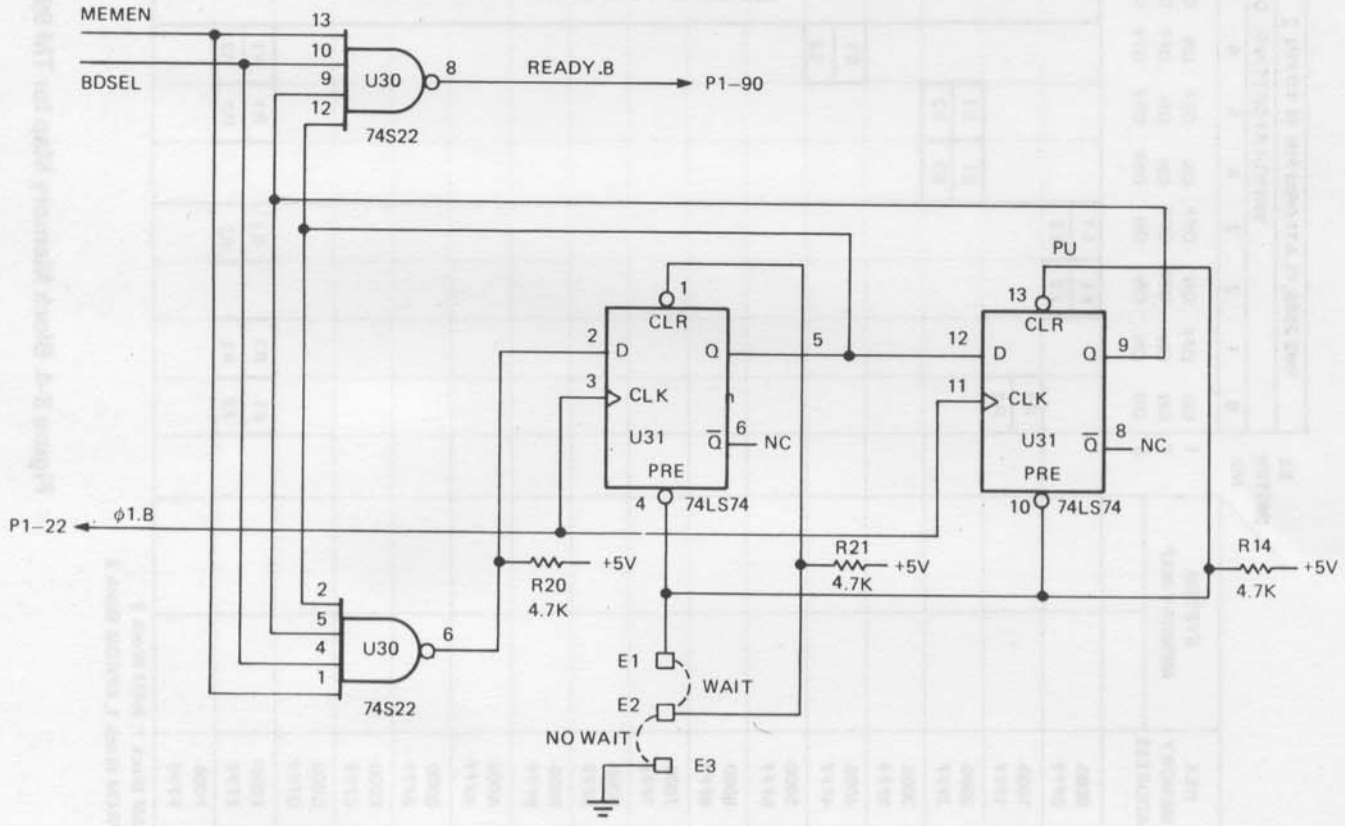


Figure 3-5. TM 990/302 Wait Logic

3.3.5 Memory Decoding

EPROM and RAM memory decoding aboard the TM 990/302 software development board is accomplished through the use of the memory decode PROM U28. U28 is a 74S287, 256 × 4 bit PROM. This PROM accepts switch and EPROM configuration platform inputs along with the address A0-A3. For any fixed switch and platform input one memory configuration is available. Since there are 16 combinations of switch and platform inputs, a total of 16 memory configurations is available. Appendix D describes how to program this chip for custom memory mapping.

The memory configurations are best described through use of Figures 3-3 and 3-4. These figures show the memory block enabled for any given input of address, switch and configuration platform. As an example assume that the switches are in position ON OFF OFF and that the 2K/4K input from the EPROM configuration platform is at a logic 1 level (tied to +5 V) then RAM memory is defined at addresses $E000_{16}$ through $EFFF_{16}$ and EPROM memory is defined at addresses 4000_{16} through $5FFF_{16}$. Also note that when 2K/4K is at a logic 1 level, 2 banks of 2K words of EPROM are defined and when 2K/4K is at a logic 0 level, 2 banks of 4K words of EPROM are defined.

2K/4K is a signal input to the decode PROM from the EPROM configuration platform that determines the amount of EPROM memory configured into the memory map. This signal originates on the EPROM configuration platform where it is hard wired to +5 V or ground. The effect of this input is to shift to one side or the other of Figure 3-3. If 2K/4K is wired to ground the left side of the figure is used. Note that 8 configurations are available for the memory when 2K/4K is ground and 8 configurations when 2K/4K is tied to +5 V. This accomodates the use of different size EPROMs.

The following EPROMs are accomodated by the TM 990/302 software development system:

Name	Configuration	Voltage Required
TMS 2508	1K × 8 bits	+5 V
TMS 2516	2K × 8 bits	+5 V
TMS 2716	2K × 8 bits	−5 V, +5 V, +12 V
TMS 2532	4K × 8 bits	+5 V

This flexibility is accomplished through the use of the EPROM configuration platform. The schematic for this platform is shown in Figure 3-6 along with the wiring for the EPROMs mentioned above. The platform corresponding to the EPROMs desired must be used. *Although the TM 990/302 accomodates these different EPROMs, they may not be mixed. For example, a TMS 2516 and TMS 2716 cannot be used on the same board.*

The memory decode logic is shown in Figure 3-7. Basically U28 outputs board select, EPROM 1 and EPROM 2 selects, and RAMEN (RAM ENABLE). This RAMEN signal is further decoded into 2 selects through the use of A4 which determines what block of RAM is to be accessed.

U19 has RAMEN, RAM and A4 as inputs. RAM is essentially an 'OR' function of DBIN and WE. This is done for timing considerations only. /SEL 1.R is driven low when A4 is a zero allowing bank 1 of RAM to be selected. Likewise when A4 is a one, the chip select for bank 2 is driven low. This indicates that bank 1 will always occupy the lower part of the 2K word block decoded by U28. The upper half will be occupied by bank 2. This is shown on Figure 3-3.

In a similar manner, the EPROM outputs are qualified by DBIN and MEMEN and sent to U25 where they are jumpered to the appropriate bank of EPROM. U24 is used in this case to guarantee that the EPROM is only accessed during a valid memory read cycle.

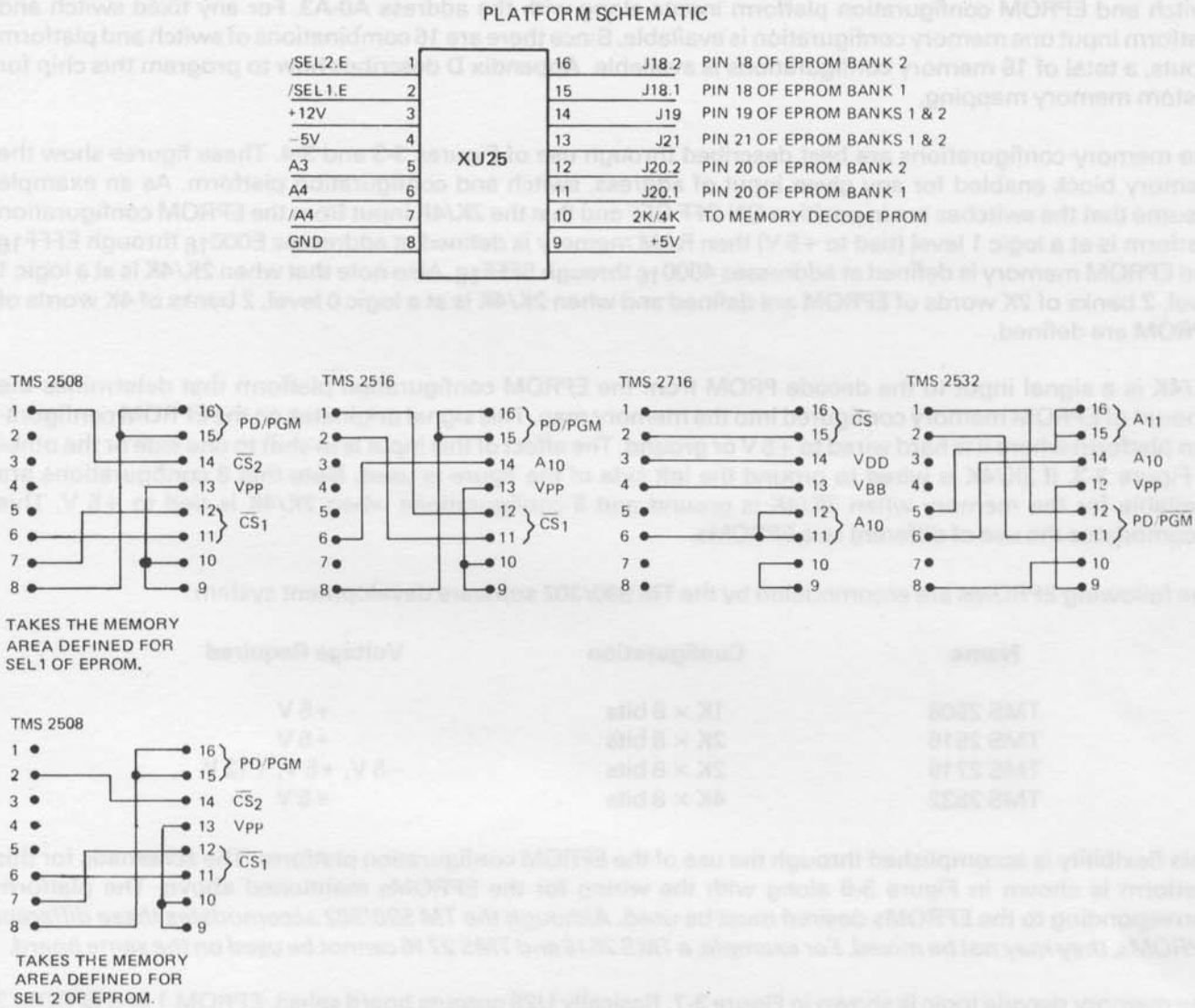


Figure 3-6. Adaptor Platforms for EPROM on TM 990/302

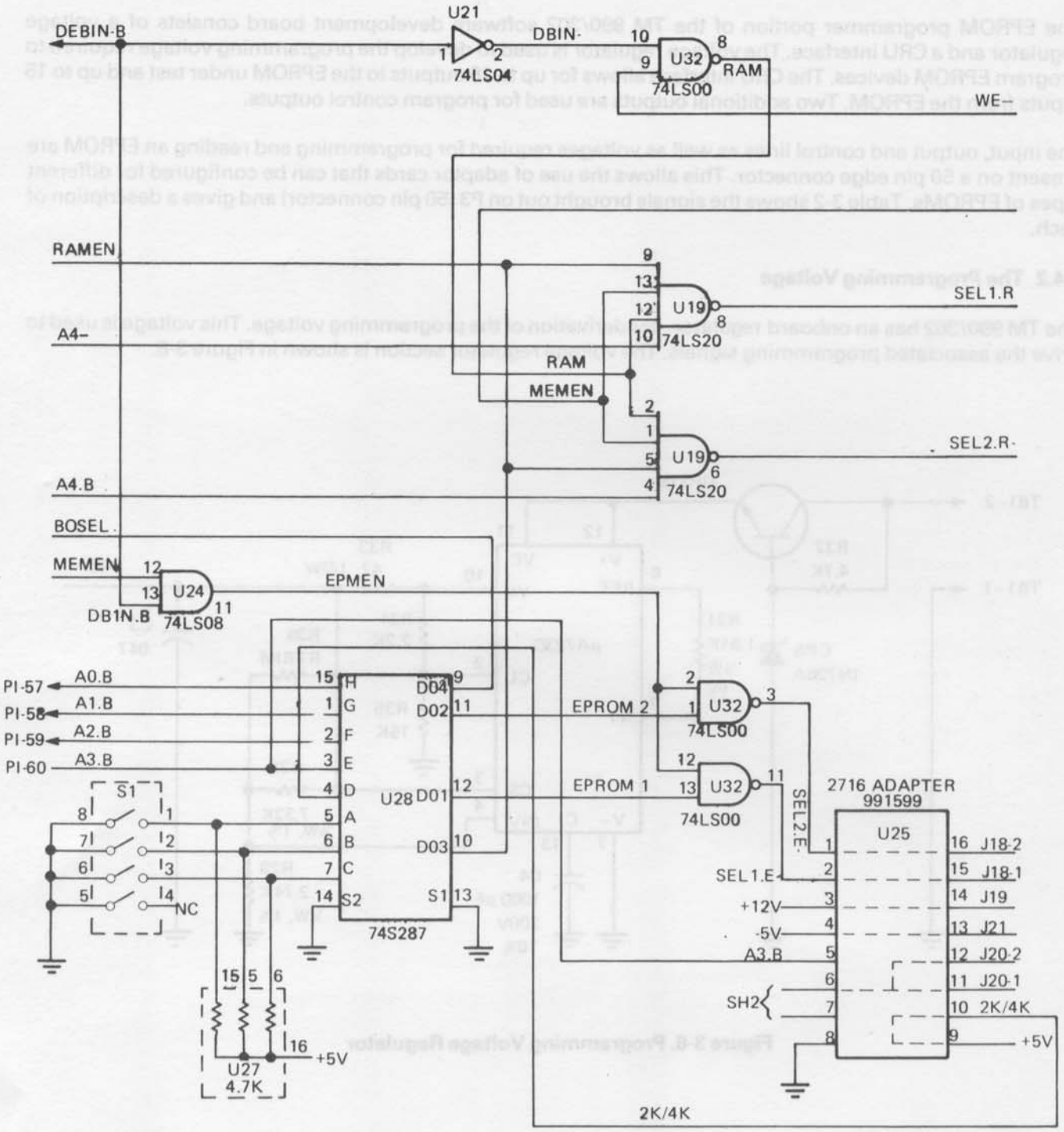


Figure 3-7. Memory Decode Logic

3.4 EPROM PROGRAMMER AND CRU INTERFACE OVERVIEW

3.4.1 EPROM Programmer

The EPROM programmer portion of the TM 990/302 software development board consists of a voltage regulator and a CRU interface. The voltage regulator is used to develop the programming voltage required to program EPROM devices. The CRU interface allows for up to 16 outputs to the EPROM under test and up to 15 inputs from the EPROM. Two additional outputs are used for program control outputs.

The input, output and control lines as well as voltages required for programming and reading an EPROM are present on a 50 pin edge connector. This allows the use of adaptor cards that can be configured for different types of EPROMs. Table 3-2 shows the signals brought out on P3 (50 pin connector) and gives a description of each.

3.4.2 The Programming Voltage

The TM 990/302 has an onboard regulator for derivation of the programming voltage. This voltage is used to drive the associated programming signals. The voltage regulator section is shown in Figure 3-8.

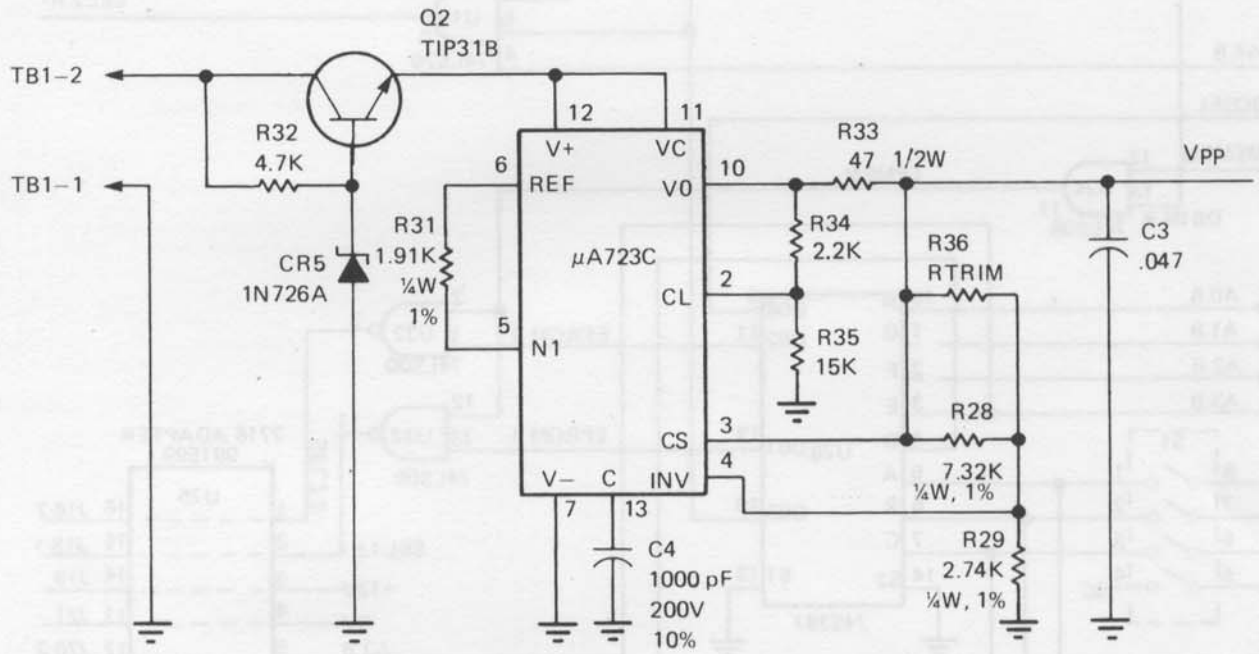


Figure 3-8. Programming Voltage Regulator

TABLE 3-2. EPROM PROGRAMMER INTERFACE

Pin #	Name	Class	Description
1	LCD0	CRU Input	Intended for use as device I. D. code in order to check jumper settings, read flags, and check that the proper board is being used. (TTL level)
2	LCD1		
3	LCD2		
4	LCD3		
5	LCD4		
6	LCD5		
7	LCD6		
8	AD0	CRU Output	Latched outputs to device under test intended for use as addresses to the device. Can be used for logic outputs. (TTL level)
9	AD1		
10	AD2		
11	AD3		
12	AD4		
13	AD5		
14	AD6		
15	AD7		
16	AD8		
17	AD9		
18	AD10		
19	AD11		
20	AD12		
21	AD13		
22	AD14		
23	AD15		
24	$\overline{\text{PGMENL}}$	Control Output	0-5 V level high when PGMEN is low
25	+5 V	Voltage	Voltage pins. These two can determine
26	Ground	Voltage	adaptor polarity. See description Sec. 2-10.
27	EPMDTA0	CRU Input-Output	Latched outputs and CRU data inputs intended for use as data drivers/receivers.
28	EPMDTA1		
29	EPMDTA2		
30	EPMDTA3		
31	EPMDTA4		
32	EPMDTA5		
33	EPMDTA6		
34	EPMDTA7		
35	V_{pp}	Voltage	25 V ±1/2 V
36	Ground	Voltage	Signal ground
37	−5 V	Voltage	V_{BB} for 27XX series EPROMs
38	$\overline{\text{PGMEN}}$	Control Output	TTL program enable
39	$\overline{\text{LEDDRV}}$	Indicator	Intended for use as LED driver to indicate program mode. Low when PGMEN is high. Open collector.
40	/PGMPLS.TTL	Control Output	Active low when program pulse is set high. This level is TTL compatible. Enabled by PGMEN.
41	Signal ground	Voltage	ground
42	+12 V	Voltage	V_{DD} for 3 supply EPROMs
43	Signal ground	Voltage	Ground
44	PGMEN.25	Program Voltage*	Driven from PGMEN. Same polarity. Level 25.5 ± 1/2 V
45	Signal ground	Voltage	Ground
46	PGMPLS.27	Program Voltage*	Driven from PGMPLS. Same polarity. Level 25.5 ± 1/2 V
47	Signal ground	Voltage	Ground
48	PGMENH	Control Voltage	Driven from and same polarity as PGMEN. High level is 12 V.
49	PGMENL	Control Voltage	Driven from and same polarity as PGMEN. High level = 5 V.
50	PGMPLS	Control Voltage	TTL level program pulse.

*Program Voltage = V_{pp} = 25.5 V ± .5 V

The voltage required for proper operation of the regulator circuit is brought onboard through TB1 (pins 1 and 2), a four position terminal strip as shown in Figure 3-8. Transistor Q2, resistor R32 and diode CR5 constitute a voltage preregulator for the voltage regulator VR2. This serves to insure that the voltage supplied to VR2 does not exceed maximum rated voltage (40V). VR2 is a uA723 adjustable voltage regulator programmed by R28, Rtrim (R36), and R29. Rtrim is selectable at test. The voltage tolerances for input and output are given in Table 3-3.

TABLE 3-3. $V_{IN(MAX)}$ AND V_{REG}

V	I_{MAX}	I_{TYP}
V_{IN} 35 - 55 V	100 mA	60 mA
V_{REG} 25 - 26 V	40 mA	—

R33 is a current sensing resistor and in conjunction with R34 and R35 provides foldback current limiting. This feature insures that the voltage regulator will shut down when a bad device is plugged into the programming socket which requires too much programming current or is shorted.

3.4.3 Communication Register Unit (CRU)

The TMS 9900 microprocessor has two different interfaces. One is a parallel interface which is comprised of the address bus and a 16 bit data bus. This data bus is bi-directional driven both by the processor and the memory devices. The other interface is the Communication Register Unit or CRU which is comprised of the same address bus and a three line CRU bus. This CRU bus is a serial interface. The serial output line (CRUOUT) is driven only by the processor, and the serial input (CRUIN) line is driven only by the addressed CRU devices. The third line of this three line bus is CRUCLK, which is used to determine whether the CRU cycle is an output or input of serial data.

When an address is present on the address bus and MEMEN is not also active, a CRU operation is assumed. Note that even if some CRU device responds to the address bus while it changes value or is in any way invalid, no harm is done because the data presented to CRUIN by the addressed device will be ignored by the processor. Because the processor will poll CRUIN only when required, CRU address decoding is simplified.

When an address is present on the address bus, MEMEN is not active and A0-A2 are all zero, the requirements are met for a CRU operation (differentiating between CRU operation and external instruction - refer to TMS 9900 Microprocessor Data Manual for more information). If during this time the CRUCLK line is pulsed a CRU output operation is being performed. It is distinct from an input operation in that CRUCLK is active during output; whereas, it is inactive upon input. CRUCLK can be used as a clock to latches in order to latch output data. A CRU input is achieved by the processor asserting an address while keeping the MEMEN signal inactive, and then polling CRUIN at the appropriate time.

The CRU outputs and inputs for the TM 990/302 are at fixed locations in the CRU address map. The CRU output functions are presented in Table 3-4 and the CRU inputs are described in Table 3-5. Note that these inputs and outputs may be used for multiple purposes. The description given in the tables is for the intended use of the functions. Note also that the same CRU address may be used for more than one function. The difference is that in one case the processor is outputting data and in the other case data is input to the processor.

TABLE 3-4. TM 990/302 CRU OUTPUT DEFINITIONS

Name	CRU Base Address (Hex Values)	Function
Recorder 1 Forward	1700	'1' output turns recorder 1 on, '0' turns recorder 1 off.
Recorder 2 Forward	1702	'1' output turns recorder 2 on, '0' turns recorder 2 off.
Recorder 2 Write Data	1704	Data is sent to the recorder through this port.
PGMEN	1706	Used to control program functions (See Table 3-2)
PGMPLS	1708	Used to control program functions (See Table 3-2)
EPMDTA 0 LSB	1710	Data to device in program socket is output through these 8 outputs.
	1712	
	1714	
	1716	
	1718	
	171A	
	171C	
EPMDTA 7	171E	
EPROM ADDRESS LSB	1720	These outputs are defined to supply the addresses to the
(AD0 - AD15)	1722	EPROM in the programming socket.
	1724	
	1726	
	1728	
	172A	
	172C	
	172E	
	1730	
	1732	
	1734	
	1736	
	1738	
	173A	
	173C	
	173C	
EPROM ADDRESS MSB	173E	

TABLE 3-5. TM 990/302 CRU INPUT DEFINITIONS

Name	CRU Base Address (Hex Values)	Function
Recorder data input	1700	Recorder input is received by inputting from this location.
LCD0	1702	Device I. D. codes used to verify the presence of the correct adaptor and
	1704	proper placement of the jumpers for different device types.
	1706	
	1708	
	170A	
	170C	
LCD6	170E	
EPROM DATA BIT O MSB	1710	Data read through CRU addresses 1710 through 171E is read from the
(EPMDTA 0 - 7)	1712	EPROM in the programming socket.
	1714	
	1716	
	1718	
	171A	
	171C	
EPROM DATA BIT 1 LSB	171E	

The CRU base addresses given are the addresses that would be loaded into register 12 in order to access the desired function. For example to set program enable in the high state the following 2 instruction sequence could be used.

```
LI R12, >1706      Load CRU base for PGMEN.
SBO 0              Set PGMEN high.
```

To set PGMEN and PGMPLS high at the same time add:

```
SBO 1              Set PGMPLS high.
```

Note that the CRU base addresses are two hex digits apart and that there is only a difference of 1 between bits set, that is because the set bit instruction shifts the operand one place to the left and adds it to the contents of R12 to form the CRU address. Shifting left 1 place has the effect of multiplying by two. Therefore the instruction SBO 1 adds 2 to 1706 and outputs a logic 1 to this address. For more information on CRU addressing see the TM 990/100M User's Manual.

3.5 AUDIO CASSETTE INTERFACE

The audio cassette interface consists of three basic units, the motor control logic, the write circuitry and the read circuitry. The motor control logic is very simple. In order to turn on the cassette drive a contact closure is required. This is done by 2 reed relays on the TM 990/302. Figure 3-9 shows the components involved. To close a contact a logic 'one' is output to the motor control bit. A logic 'zero' opens the contact and when open the cassette drive is turned off.

U39 is an addressable latch used to hold the data written to locations >1700 through >1708. Outputting a 'one' to CRU address >1700 sets RECFWDO to a high level. The 7406 (U35) inverts this signal and pulls its output low. This applies 12 V to the relay coil. This turns the relay on and the circuit is closed allowing the cassette to start. The same is true for recorder 2 motor control.

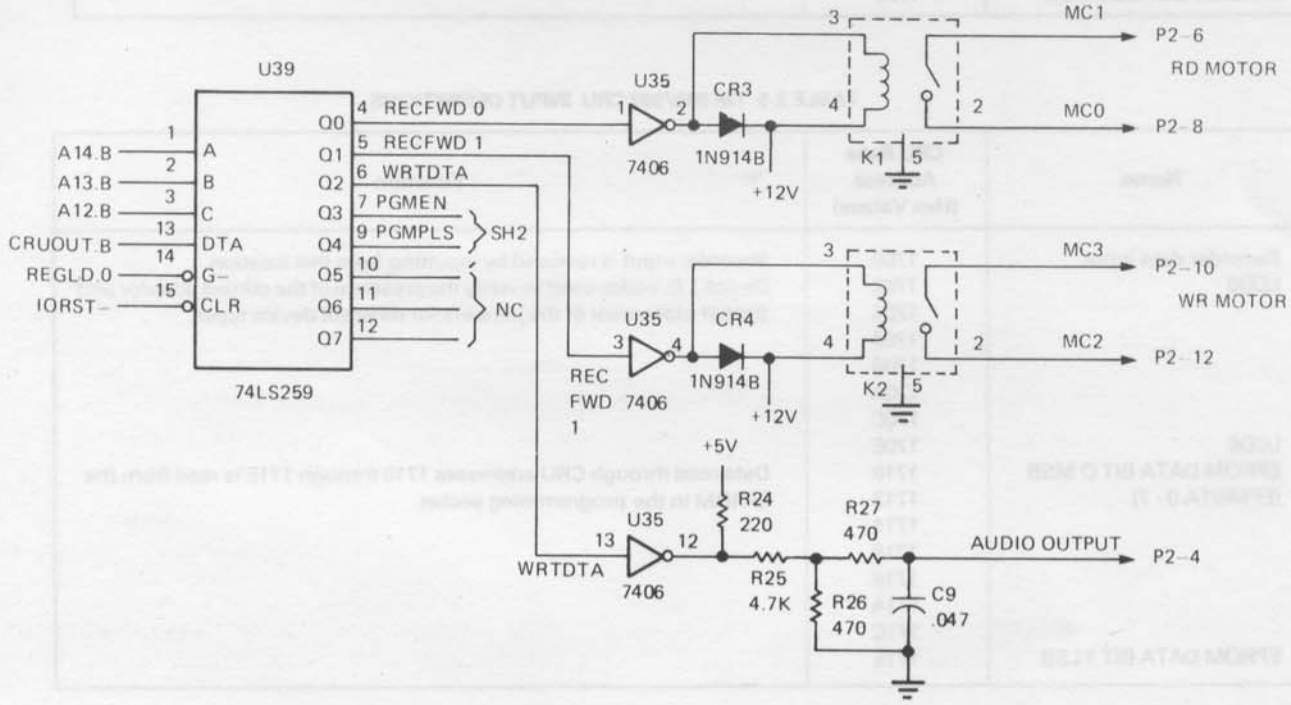


Figure 3-9. Motor Control and Write Circuitry

The write circuitry is also shown in Figure 3-9. Basically a bit written to CRU base address >1704 is buffered by U39. U35 allows the signal to swing to a known voltage range 0 - 5 V. R24 supplies the pull up. R25 and R26 divide the 5 V signal by 10 producing a new signal that swings 0 - 500 mV. Finally the signal is sent through a low pass filter consisting of R27 and C9 that attenuates the high frequencies making it acceptable for the recorder.

For detection of the stored data the circuit shown in Figure 3-10 is used. The input from the earphone output is ac coupled to the first stage of a two stage buffer. The first stage clips the incoming waveform in order to recondition the wave and restore the basic period fo the stored signal. This output is fed into the second stage which amplifies the signal in order for it to be detected. U33, a 75189A line receiver is used for detection of this signal and converts the signal to a signal that is TTL compatible. Finally U42 is used to drive the CRU interface input line (CRUIN). Notice that U42 is also used for input of the device ID codes LCD0-LCD6. U42 is a 74LS251 addressable decoder that allows CRU samplings of the data from cassette.

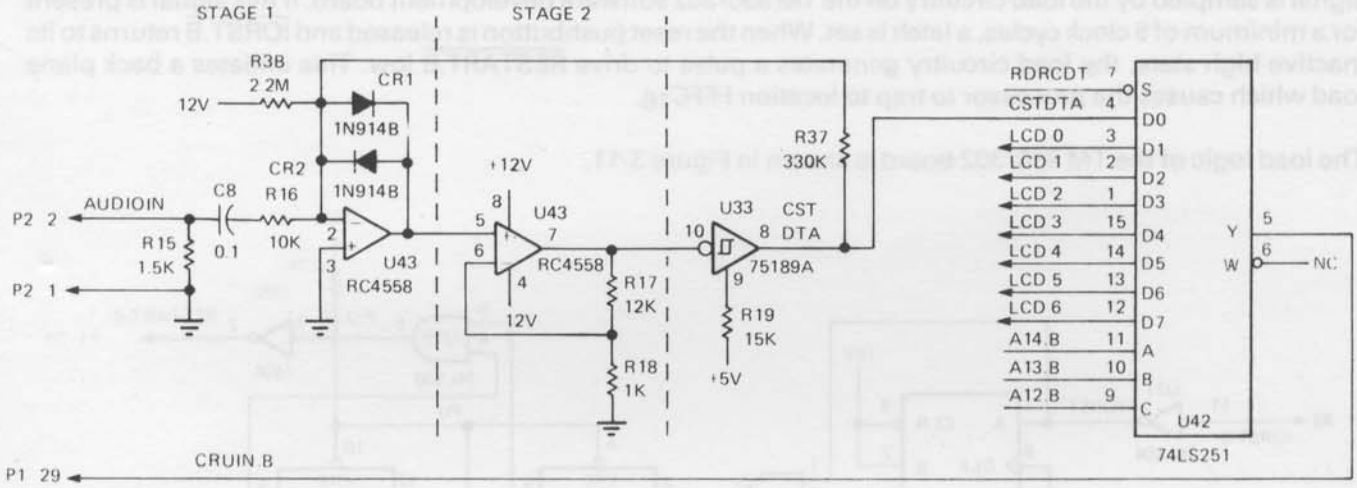


Figure 3-10. Read Circuitry

3.6 INITIALIZATION

3.6.1 RESET

There are two methods of initializing a TMS 9900 system. (That is a system based on the TMS 9900.) One method is to present a $\overline{\text{RESET}}$ signal to pin 6 of the processor. This causes the processor to trap to vectors at location 0000_{16} and location 0002_{16}. Location 0000_{16} contains the address of the workspace registers and location 0002_{16} contains the program counter.

Trapping to location 0000_{16} means only that the processor reads the data at location 0000_{16} and sets its workspace pointer from the results of the read. Likewise a read at location 0002_{16} is done to pick up the program counter. The processor then starts execution at the location indicated by the contents of memory location 0002_{16}.

3.6.2 LOAD

Initializing the TMS 9900 with a $\overline{\text{LOAD}}$ pulse on pin 4 is much the same. Except the processor this time traps to vectors at high memory; locations $FFFC_{16}$ an $FFFE_{16}$ to pick up the workspace pointer and program counter.

The method of initializing the processor becomes a question of system configuration. Whether non-volatile memory is located at high or low memory addresses is quite significant. For example, a system configured with EPROM at low memory (location 0000_{16}) and RAM at high memory, would need a $\overline{\text{RESET}}$ pulse to initialize program execution. The EPROM in this case would store the reset vectors. On the other hand if the system was configured such that EPROM was resident at high memory a $\overline{\text{LOAD}}$ pulse would be required to insure proper initialization of program execution.

Refer to the TMS 9900 Microprocessor Data Manual, and the TM 990/101M or TM 990/100M Microcomputer User's Guide for more information on reset and load.

3.7 LOAD LOGIC

A RESET is done on the TM 990/100M or TM 990/101M microcomputer boards by actuating the RESET switch on the PC board. This generates an $\overline{\text{IORST.B}}$ signal on the backplane that is used to reset I/O devices. This signal is sampled by the load circuitry on the TM 990/302 software development board. If this signal is present for a minimum of 5 clock cycles, a latch is set. When the reset pushbutton is released and $\overline{\text{IORST.B}}$ returns to its inactive high state, the load circuitry generates a pulse to drive $\overline{\text{RESTART.B}}$ low. This initiates a back plane load which causes the processor to trap to location $FFFC_{16}$.

The load logic of the TM 990/302 board is shown in Figure 3-11.

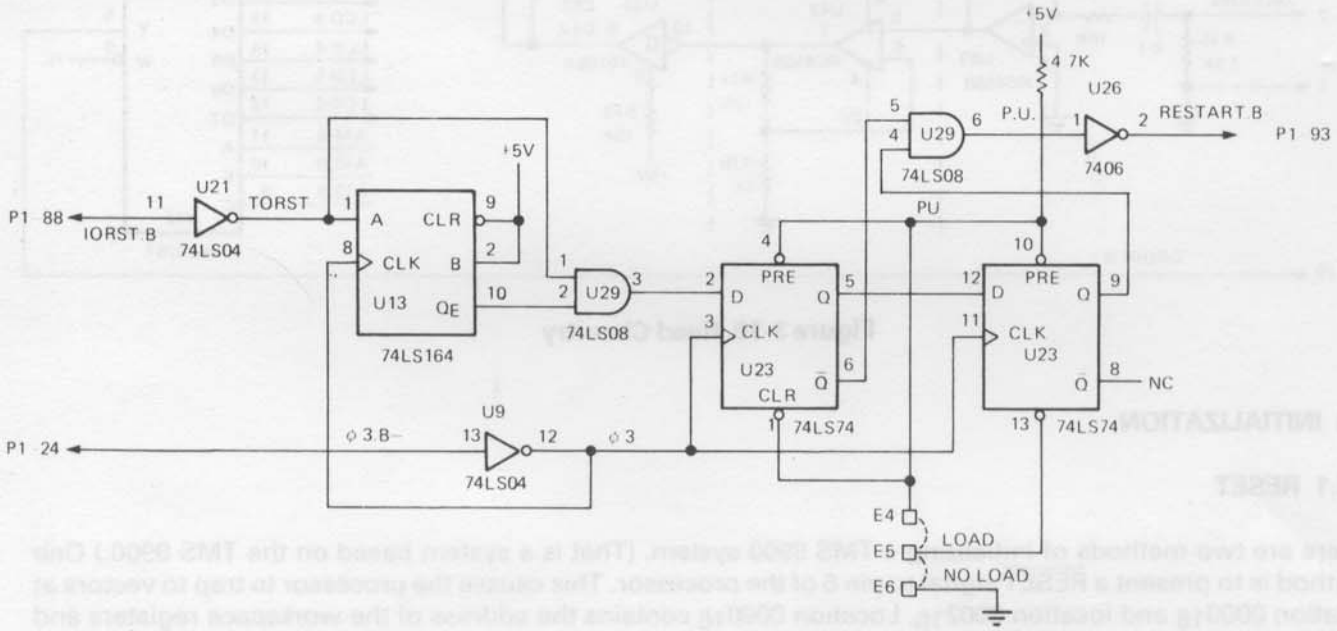


Figure 3-11. Load Logic

IORST.B is input from the backplane. This signal is active low where the reset pushbutton on the processor is being held, PRES.B is held low, or a RSET instruction is being performed.

It is only during the system resets (PRES.B is low) (or the reset pushbutton is held) that we may want to generate a load. Only when IORST is high for 5 clock cycle does the output of U29 (pin 3) go high. This filters out the time when a RSET instruction is active because IORST is only active for 2 clock cycles in this case. For more on IORST.B see the TM 990/100M Microcomputer Users Guide.

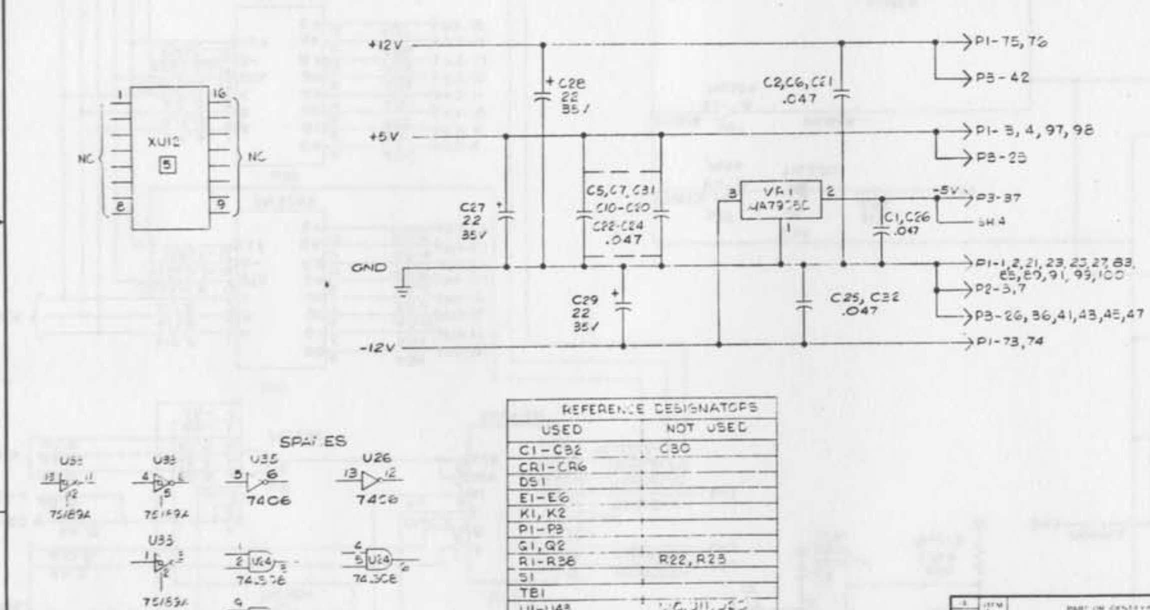
U23, a 74LS74 acts as a negative going edge detector. It is when the operator releases the RESET pushbutton and allows the processor to run that a RESTART.B signal is generated. This forces the processor to trap to location $FFFC_{16}$. Releasing the pushbutton generated 1 pulse that is 1 clock cycle long.

APPENDIX A

SCHEMATICS

NOTES: UNLESS OTHERWISE SPECIFIED
1. CAPACITANCE VALUES ARE IN MICROFARADS
2. RESISTANCE VALUES ARE IN OHMS
3. ALL RESISTORS ARE 1/4 W, 5%
4. NC DENOTES NO CONNECTION
[5] SOCKET AT XU12 IS PROVIDED FOR SHIPMENT OF A SPECIAL PROM, TO BE USED ON ANOTHER ASSEMBLY IN CONJUNCTION WITH THIS ASSEMBLY
[6] R36 VALUE SELECTED AT UNIT TEST

REFERENCE DESIGNATORS	DEVICES	-12 V	-5 V	GND	+5 V	+12 V
U14 - U17	TMS 2716			12	24	
U34	MPQ2907					
U1 - U8	TMS 4045			9	18	
U40	74LS241			10	20	
[illegible]	74S287			8	16	
U36 - U39	74LS259			8	16	
U41, U42	74LS251			8	16	
U22	74LS138			8	16	
U32	74LS00			7	14	
U9, U21	74LS04			7	14	
U26, U35	7406			7	14	
U24, U29	74LS00			7	14	
U13	74LS164			7	14	
U30	74S22			7	14	
U19	74LS27			7	14	
U18	74LS30			7	14	
U23, U31	74LS74			7	14	
U33	75189A			7	14	
U43	RC4558P	4				8



REFERENCE DESIGNATORS	
USED	NOT USED
C1-C32	C30
CR1-CR6	
DS1	
E1-E6	
K1, K2	
P1-P8	
Q1, Q2	
R1-R38	R22, R23
S1	
TB1	
U1-U43	U6, U11, U20
VR1, VR2	
XU12, XU13	

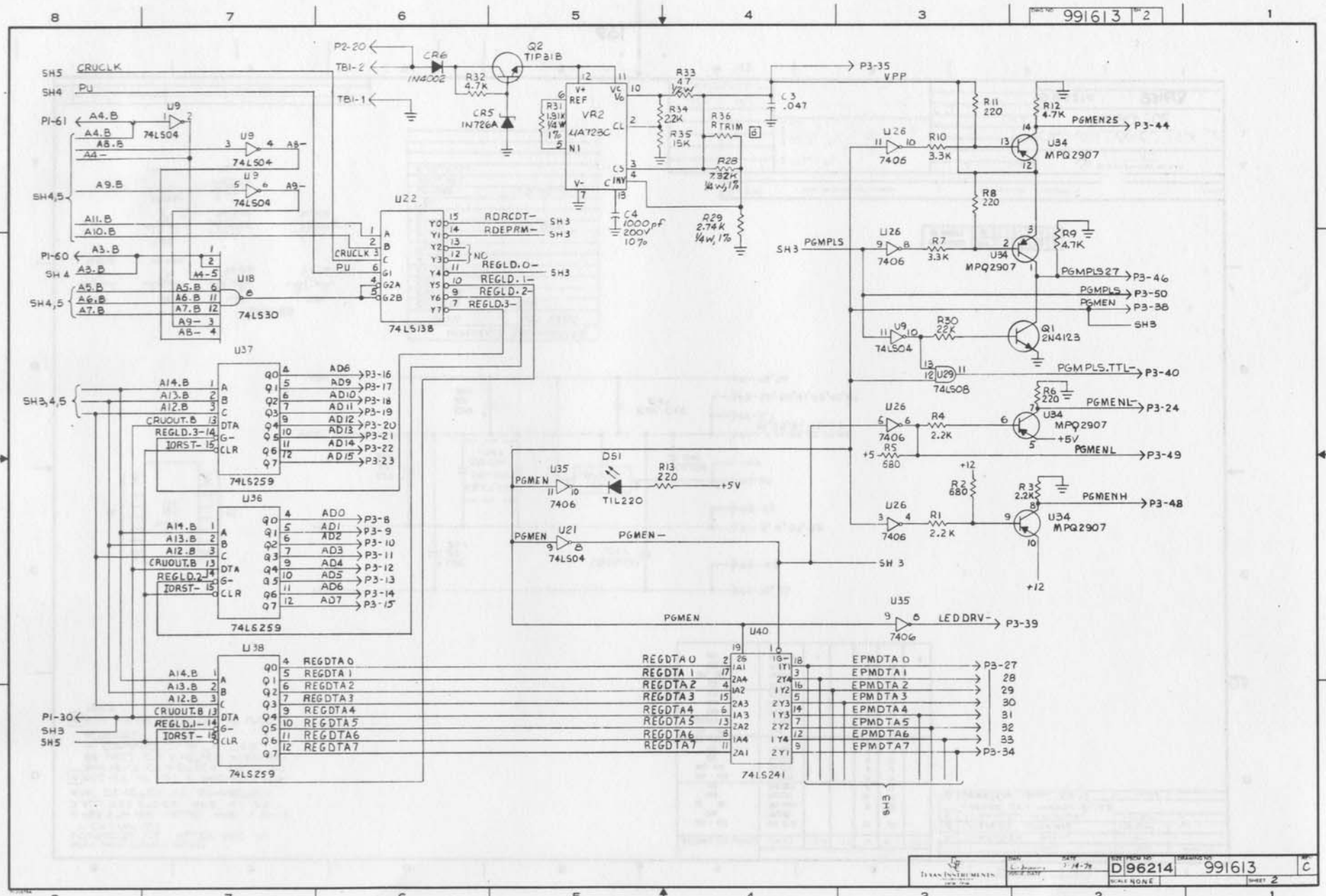
REV STATUS OF SHEETS	REV	C	C	D	B	A
	SH	1	2	3	4	5

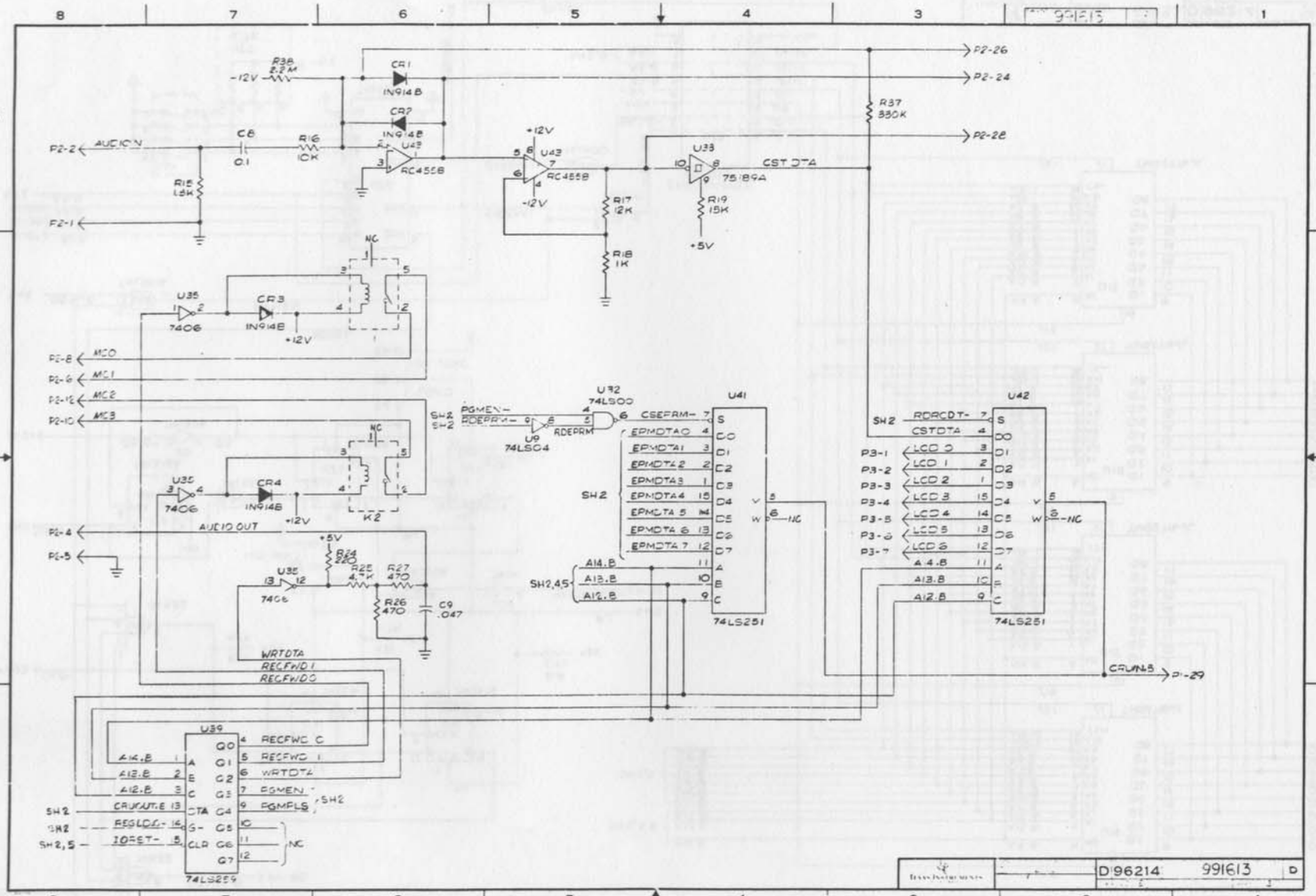
TEXAS INSTRUMENTS

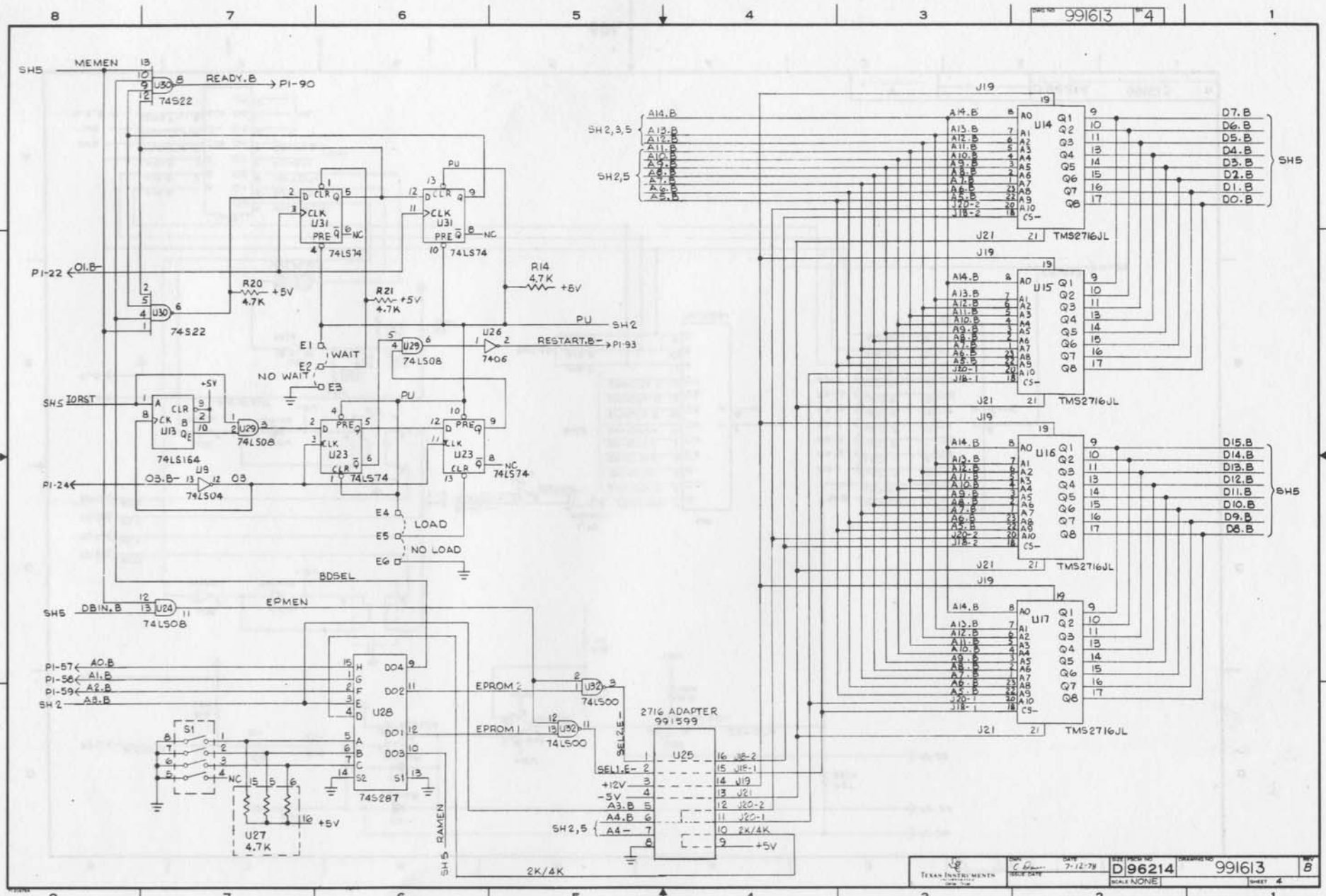
DIAGRAM, LOGIC, DETAILED TM990/302

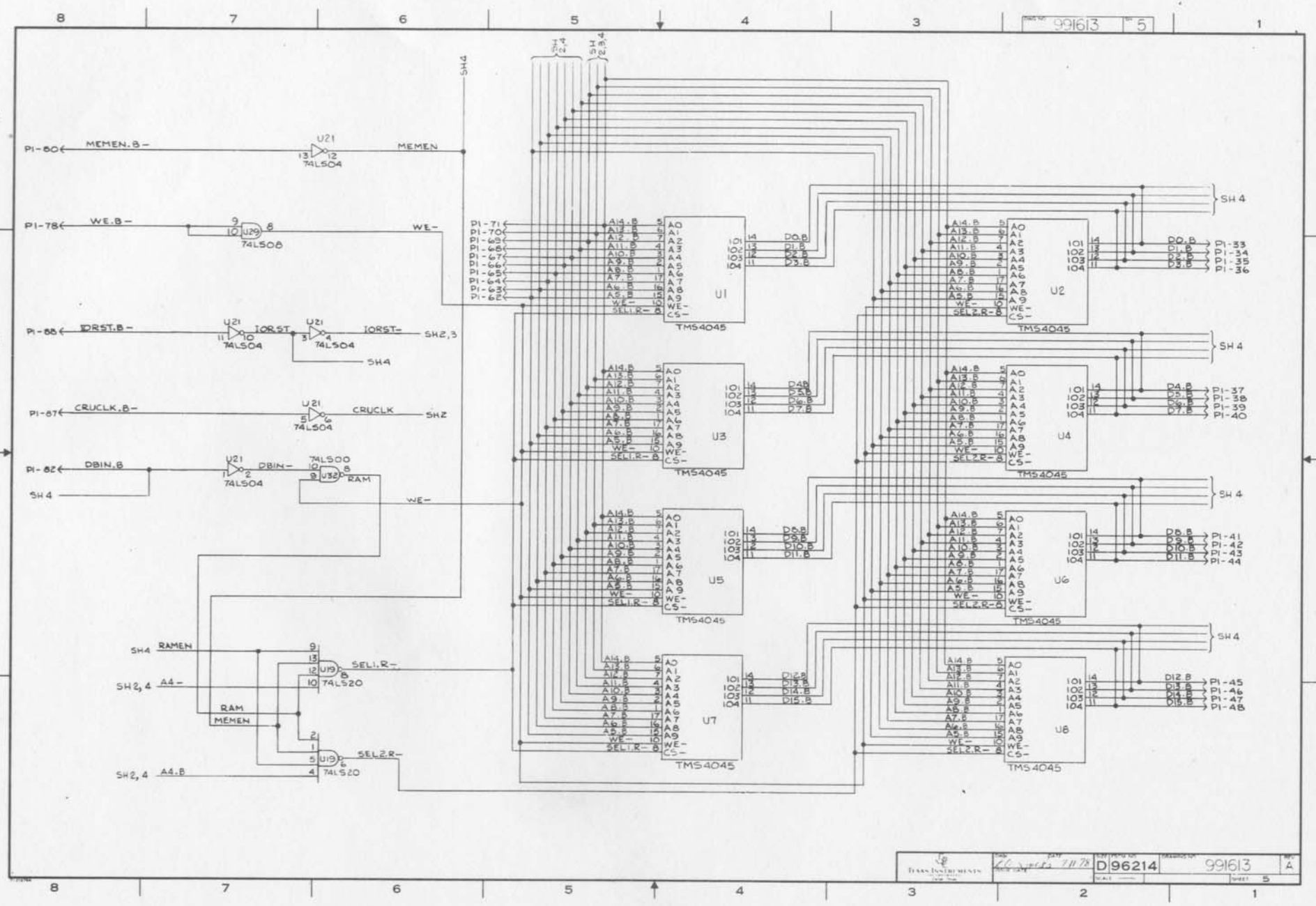
D 96214 991613

691


991613 2
P2-20
TBI-2
TBI-1
CR6
IN4002
Q2
TIP31B
R32
4.7K
CR5
IN726A
VR2
UA723C
R31
1.91K
1/4W
1%
R33
47
1/2W
R34
22K
R35
15K
R36
RTRIM
R28
732K
1/8W 1%
R29
2.74K
1/4W, 1%
C3
.047
C4
1000pf
200V
10%
P3-35
VPP
R11
220
R12
4.7K
PGMEN25
P3-44
U34
MPQ2907
U26
7406
R10
3.3K
R8
220
R9
4.7K
PGMPLS27
P3-46
R7
3.3K
PGMPLS
P3-50
PGMEN
P3-38
SH3
SH3
PGMPLS
R30
22K
Q1
2N4123
U9
74LS04
U29
74LS08
PGMPLS.TTL-
P3-40
R6
220
PGMENL-
P3-24
R4
2.2K
+5V
R5
680
PGMENL
P3-49
+12
R2
680
R3
2.2K
PGMENH
P3-48
R1
2.2K
+12
U35
7406
LEDDRV-
P3-39
DS1
TIL220
R13
220
+5V
U21
74LS04
PGMEN-
SH3
PGMEN
U40
74LS241
REGDTA0
REGDTA1
REGDTA2
REGDTA3
REGDTA4
REGDTA5
REGDTA6
REGDTA7
EPMDTA0
EPMDTA1
EPMDTA2
EPMDTA3
EPMDTA4
EPMDTA5
EPMDTA6
EPMDTA7
P3-27
28
29
30
31
32
33
P3-34
U22
74LS138
CRUCLK
PU
RDRCDT-
RDEPRM-
REGLD.0-
REGLD.1-
REGLD.2-
REGLD.3-
NC
U18
74LS30
U37
U36
U38
74LS259
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
P3-8
P3-9
P3-10
P3-11
P3-12
P3-13
P3-14
P3-15
P3-16
P3-17
P3-18
P3-19
P3-20
P3-21
P3-22
P3-23
CRUOUT.B
IDRST-
PI-61
PI-60
PI-30
SH5
SH4
SH4,5
SH3,4,5
D96214
991613
C
SHEET 2


991613
P2-26
P2-24
P2-28
R38 2.2M
-12V
CR1 IN914B
CR2 IN914B
P2-2 AUDIO IN
C8 0.1
R16 10K
U43 RC4558
R15 15K
P2-1
+12V
U43 RC4558
-12V
R37 330K
U33 75189A
CST DTA
R17 12K
R19 15K
+5V
R18 1K
NC
U35 7406
CR3 IN914B
+12V
P2-8 MC0
P2-9 MC1
P2-12 MC2
P2-10 MC3
U32 74LS00
PGMEN-
RDEPRM-
U9 74LS04
RDEPRM
CSEEPRM-
U41
EPMDTA0
EPMDTA1
EPMDTA2
EPMDTA3
EPMDTA4
EPMDTA 5
EPMDTA 6
EPMDTA 7
SH2
A14.B
A13.B
A12.B
SH2,4,5
74LS251
NC
U42
SH2
RDRCDT-
CSTDTA
P3-1 LCD 0
P3-2 LCD 1
P3-3 LCD 2
P3-4 LCD 3
P3-5 LCD 4
P3-6 LCD 5
P3-7 LCD 6
74LS251
CRUN&S
P1-29
U35 7406
CR4 IN914B
+12V
K2
P2-4 AUDIO OUT
P2-5
+5V
R24 220
R25 47K
R27 470
R26 470
C9 .047
U35 7406
WRTDTA
RECFWD1
RECFWD0
U39
A14.B
A13.B
A12.B
SH2
CRUNAUT.E
SH2
REGLOC-
SH2,5
IOFST-
CTA
G-
CLR
PGMPLS
RECFWD 0
RECFWD 1
WRTDTA
PGMEN
NC
74LS259
D96214
991613
D


991613 4
SH5
MEMEN
U30
74S22
READY.B
PI-90
PI-22
01.B
R20
4.7K
+5V
R21
4.7K
+5V
R14
4.7K
+5V
PU
SH2
U31
74LS74
U30
74S22
E1
WAIT
E2
NO WAIT
E3
U29
74LS08
U26
7406
RESTART.B
PI-93
SH5
IORST
U13
74LS164
+5V
U29
74LS08
U23
74LS74
U9
03.B
74LS04
PI-24
03
E4
LOAD
E5
NO LOAD
E6
BDSEL
SH5
DBIN.B
U24
74LS08
EPMEN
PI-57
PI-58
PI-59
SH2
A0.B
A1.B
A2.B
A3.B
U28
74S287
S1
U27
4.7K
+5V
SH5 RAMEN
EPROM 2
EPROM 1
U32
74LS00
SEL2.E
2716 ADAPTER
991599
U25
SEL1.E-
+12V
-5V
A3.B
A4.B
A4-
SH2,5
2K/4K
+5V
SH2,3,5
SH2,5
A14.B
A13.B
A12.B
A11.B
A10.B
A9.B
A8.B
A7.B
A6.B
A5.B
J19
J21
U14
U15
U16
U17
TMS2716JL
D7.B
D6.B
D5.B
D4.B
D3.B
D2.B
D1.B
D0.B
D15.B
D14.B
D13.B
D12.B
D11.B
D10.B
D9.B
D8.B
SH5
TEXAS INSTRUMENTS
D96214
991613
B
SCALE NONE
SHEET 4


991613
5
MEMEN.B-
MEMEN
U21
74LS04
WE.B-
WE-
U29
74LS08
IORST.B-
IORST
IORST-
SH2,3
SH4
CRUCLK.B-
CRUCLK
SH2
DBIN.B
DBIN-
74LS00
U32
RAM
RAMEN
SELI.R-
U19
74LS20
A4-
SH2,4
MEMEN
SEL2.R-
A4.B
TMS4045
U1
U2
U3
U4
U5
U6
U7
U8
P1-71
P1-70
P1-69
P1-68
P1-67
P1-66
P1-65
P1-64
P1-63
P1-62
P1-33
P1-34
P1-35
P1-36
P1-37
P1-38
P1-39
P1-40
P1-41
P1-42
P1-43
P1-44
P1-45
P1-46
P1-47
P1-48
D96214
991613
A-7/A-8

APPENDIX B

PARTS LIST

TABLE B-1. PARTS FOR TM 990/302

Symbol	Description
C1-C3, C5-C7, C9-C26, C31, C32	Capacitor .047 uF
C4	Capacitor .001 uF
C8	Capacitor 10 uF
C27-C29	Capacitor 22 uF
CR1-CR4	Diode, IN 914B
CR5	Diode, IN 726A
DS1	Diode (L.E.D., CM 4-43)
E1-E6	Pin, .025 Square
J1, J2	Jumper Plug, Connector Black
K1, K2	Relay, 12 V
Q1	Transistor, NPN, 2N4123
Q2	Transitor, TIP 31B
R1, R3, R4	Resistor, 2.2K Ohm
R2, R5, R35	Resistor, 680 Ohm
R6, R8, R11, R13, R24	Resistor, 220 Ohm
R7, R10	Resistor, 3.3K Ohm
R9, R12, R14, R20, R21, R25, R32	Resistor, 4.7K Ohm
R15	Resistor, 1.5K Ohm
R16	Resistor, 10K Ohm
R17	Resistor, 12K Ohm
R18	Resistor, 1K Ohm
R19, R35	Resistor, 15 Kilohm
R26, R27	Resistor, 470 Ohm
R30	Resistor, 22K Ohm
R33	Resistor, 47 Ohm
R34	Resistor, 150 Ohm
R37	Resistor, 330K Ohm
R38	Resistor, 2.2M Ohm
R28	Resistor, 7.32K Ohm 1%
R29	Resistor, 2.74K Ohm 1%
R31	Resistor, 1.91K Ohm 1%
S1	Switch, Dual In Line, 4 Position
TB1	Barrier, Terminal Board
U1-U8	IC, 2114 RAM
U9,U21	Network, SN74LS04N
U12	PROM, Memory Decode
U13	Network, SN74LS164N
U14-U17	IC, TMS 4045-45NL
U18	Network, SN74LS30N
U19	Network, SN74LS20N
U22	Network, SN74LS138N
U23,U31	Network, SN74LS74N
U24,U29	Network, SN74LS08N
U26,U35	Network, SN7406N
U27	Resistor, Fixed-Array 4.7K Ohm
U30	Network, SN74S22N
U32	Network, SN74LS00N
U33	Network, SN75189AN
U34	Transistor, MPQ2907
U36,U37,U38,U39	IC, SN74LS259N
U40	IC, SN74LS241N
U41,U42	Network, SN74LS251N
U43	IC, RC4558P
VR1	IC, UA7905C/MC7905CP
VR2	Network, SN72723N
XU1-XU8	Socket, 18 Pin IC
XU12,XU25,XU28	Socket, 16 Pin IC
XU14-XU17	Socket, 24 Pin IC

TABLE B-2. PARTS FOR TM 990/514 EPROM PERSONALITY MODULE

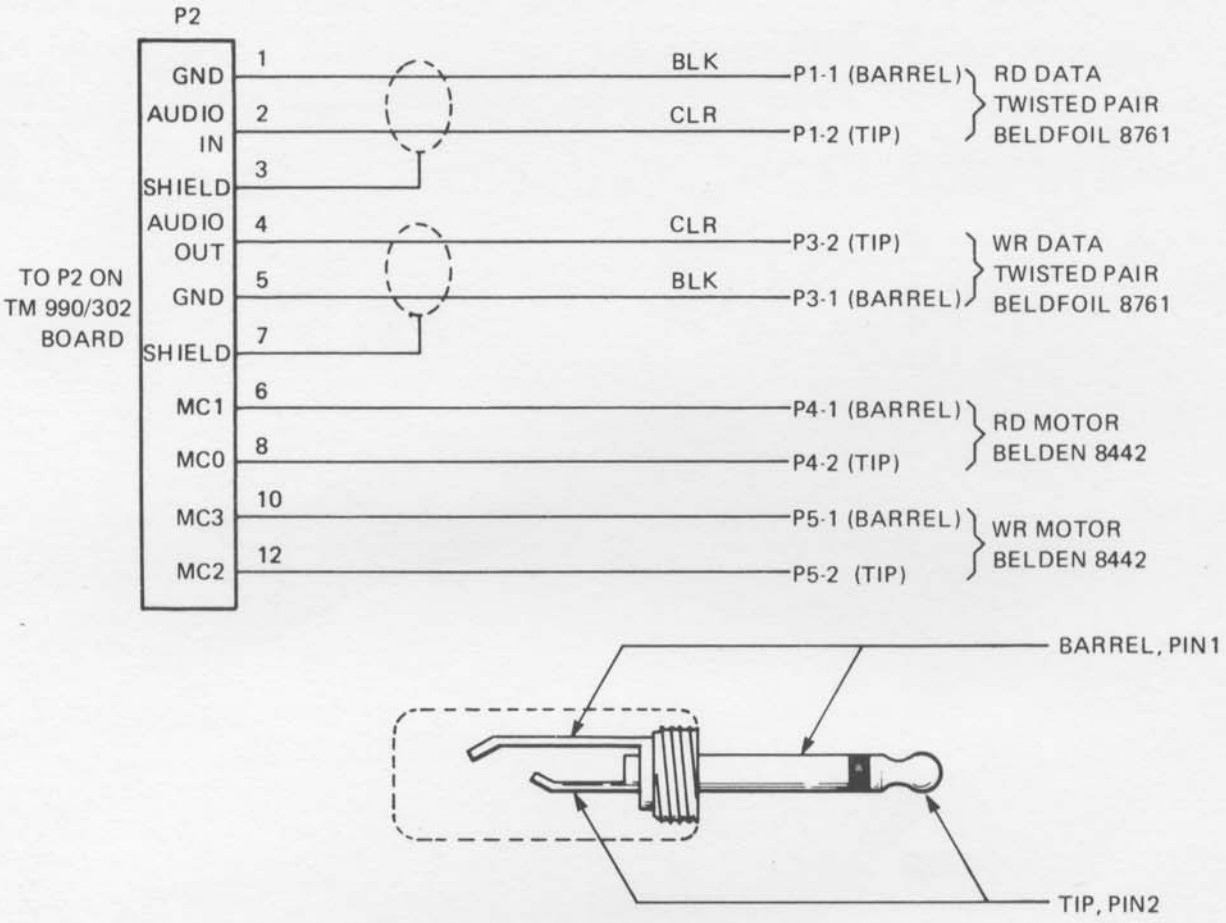
Symbol	Description
C1-C3	Capacitor, .047 uF
DS1,DS2	Diode (L.E.D., CM4-43)
E1-E9	Pin, .025 Square
P3	Connector
R1	Resistor, 4.7K Ohm
R2,R3	Resistor, 220 Ohm
XU1	DIP Socket

TABLE B-3. PARTS FOR TM 990/515 EPROM PERSONALITY MODULE

Symbol	Description
C1	Capacitor, .047 uF
DS1,DS2	Diode (L.E.D., CM 4-43)
E1-E9	Pin, .025 Square
P3	Connector
R1	Resistor, 4.7K Ohm
R2,R3	Resistor, 220 Ohm
XU1	DIP Socket

APPENDIX C

SCHEMATIC OF CABLE TM 990/508 BETWEEN AUDIO CASSETTES AND TM 990/302 BOARD



CABLE PLUG	AUDIO CASSETTE SOCKET
RD DATA	EAR or MONITOR
WR DATA	AUX
RD MOTOR	REM
WR MOTOR	REM

CAUTIONS

1. Do not plug the AUX input and EAR output plugs into the same recorder at the same time as this may cuase ground loop problems with some recorders.

2. Do not input a plug into the MIC socket.

APPENDIX D

PROGRAMMING THE MEMORY DECODE PROM

D.1 GENERAL

A memory decode PROM on the TM 990/302 board decodes address line inputs and switch S1 settings to determine which banks of EPROM to enable or if RAM should be enabled. This PROM, a 74S287 located in socket U28, can be replaced with a PROM programmed to the user's requirements. Programming requirements for this PROM are discussed in this appendix.

D.2 PROM ARCHITECTURE

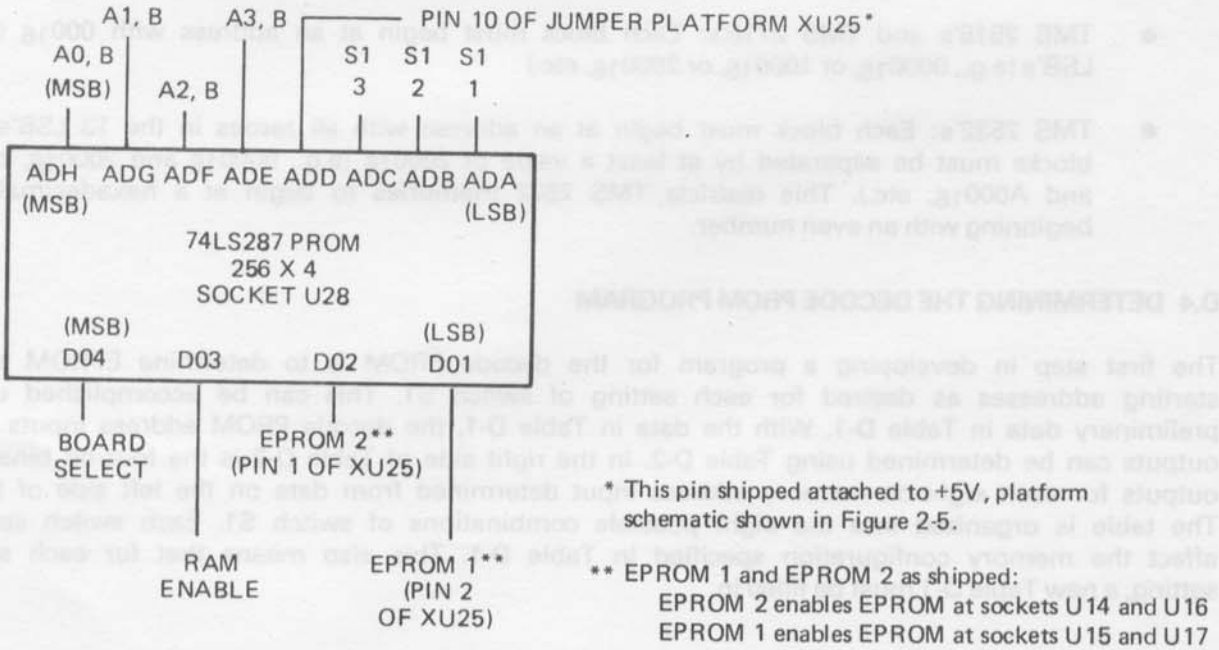
The PROM inputs and outputs are shown in Figure D-1. The four most-significant bits (MSB's) of the PROM address input lines are the four most-significant lines of the address bus, A0 to A3. The four least-significant bits (LSB's) of the PROM address input lines are one line from pin 10 of the jumper platform at XU25 and the three settings of DIP switch S1 (settings 3, 2, and 1 with setting 1 the LSB). These eight inputs contain the binary address to the 256 nibbles (half bytes or four bits) output by the PROM.

The four-bit output is as follows (see Figure D-1):

- D04 (MSB): A one enables the READY circuitry to the processor.
- D03: A one enables the onboard RAM; thus, it must be a one when addressing RAM or a zero when addressing EPROM.

CAUTION

It is important that address decoding prevent the simultaneous enabling of different memory areas, remember that this includes memory on the TM 990/302 board as well as on the microcomputer board.



* This pin shipped attached to +5V, platform schematic shown in Figure 2-5.

** EPROM 1 and EPROM 2 as shipped:
EPROM 2 enables EPROM at sockets U14 and U16
EPROM 1 enables EPROM at sockets U15 and U17

Figure D-1. Decode PROM Schematic

- D02: A one enables EPROM through pin 1 of jumper platform XU25; this pin is shipped from the factory connected to pin 16 of the platform which goes to chip selects for EPROM sockets U14 and U16.

- D01 (LSB): A one enables EPROM through pin 2 of jumper platform XU25; this pin is shipped from the factory connected to pin 15 of the platform which goes to chip selects for EPROM sockets U15 and U17.

NOTE

This appendix assumes that the U25 jumper platform will be wired for one of the different EPROM's as shown in Figure 2-5.

The programming of the PROM requires that the user decide the most significant four address line values (address space at which hardware will enable the memory when requested by software), the S1 switch settings, and the logic from pin 10 of the jumper platform for each of the two EPROM banks and for the RAM area.

D.3 CONSIDERATIONS

Onboard RAM is contained in two 1K × 16 memory blocks with Block 2 (U2, U4, U6, and U8) enabled by address line A4 (address 0800_{16}) being a one and Block 1 (U1, U3, U5, and U7) enabled by A4 being a zero; thus RAM must be addressed so that address line A4 can be used to select between blocks. Thus RAM blocks will begin at memory addresses ending in 800_{16} or 000_{16} (e.g., 1000_{16} and 1800_{16}). RAM blocks should be presented as continguous with the most significant four bits (inputs to the decode PROM) being the same number.

Blocks of TMS 2508 EPROM have to be contiguous; however this is not necessary for TMS 2516's, TMS 2716's, and TMS 2532's.

- TMS 2508's: One block must begin at an address with 000_{16} in the 12 LSB's; the second block will be contiguous starting 800_{16} bytes later (e.g., 1000_{16} and 1800_{16}).

- TMS 2516's and TMS 2716's: Each block must begin at an address with 000_{16} in the 12 LSB's (e.g., 0000_{16}, or 1000_{16}, or 2000_{16}, etc.)

- TMS 2532's: Each block must begin at an address with all zeroes in the 13 LSB's and the blocks must be separated by at least a value of 2000_{16} (e.g., 0000_{16} and 2000_{16}, or 6000_{16} and $A000_{16}$, etc.). This restricts TMS 2532 memories to begin at a hexadecimal address beginning with an even number.

D.4 DETERMINING THE DECODE PROM PROGRAM

The first step in developing a program for the decode PROM is to determine EPROM and RAM starting addresses as desired for each setting of switch S1. This can be accomplished using the preliminary data in Table D-1. With the data in Table D-1, the decode PROM address inputs and data outputs can be determined using Table D-2. In the right side of Table D-2 is the four-bit binary PROM outputs for each eight-bit memory address input determined from data on the left side of the table. The table is organized into the eight possible combinations of switch S1. Each switch setting can affect the memory configuration specified in Table D-1. This also means that for each switch S1 setting, a new Table D-1 must be filled in.

When Table D-2 is filled in properly, the decode PROM can be programmed with the four-bit half-bytes (nibbles) on the right programmed at the addresses shown in the eight-bit section on the left. Nibbles not shown on the table must be programmed with all zeroes.

TABLE D-1. DATA REQUIRED TO DETERMINE PROM CONTENTS

1. MEMORY START ADDRESS (hexadecimal):

   a. EPROM

      TMS 2508 First Block $\_\underline{0}\underline{0}\underline{0}_{16}$
      Other First Block $\_\underline{0}\underline{0}\underline{0}_{16}$ Second Block $\_\underline{0}\underline{0}\underline{0}_{16}$

   b. RAM: First Block $\_\underline{0}\underline{0}\underline{0}_{16}$

   NOTE
   "First and second block" do not necessarily pertain to Blocks 1 and 2 in Figure 2-7.

2. LOGIC WIRED TO PIN 10 OF JUMPER PLATFORM U25. _One _Zero

3. SWITCH S1 SETTING (enter 1 for OFF, and 0 for ON):

   No. 3__ No. 2__ No. 1__

Note that for the switch S1 settings, a ON causes a zero and OFF causes a one to be applied to the decode PROM address inputs. Also, if TMS 2532's are used, a zero must be applied to address line A3 (input ADE) of the decode PROM, and this will be the entry on Table D-2 (fourth column at top of table).

The fifth column of Table D-2 is the logic value at pin 10 of jumper socket U25. This is tied to a logic zero for EPROM type TMS 2532 and to zero for all other types. This socket is shown in Figure 2-5.

To use these tables, do the following:

(1) Fill in Table D-1 with data for a particular switch S1 setting.

(2) Find on Table D-2 the three lines pertaining to the switch setting shown in step 3 of Table D-1.

(3) In the left side of Table D-2, fill in the binary value of the MSB of the address shown for both EPROM blocks and the RAM block (a TMS 2508 memory requires only the start address of the block). E1 is the start address of EPROM Block 1, and E2 is the start address of EPROM Block 2.

(4) For other settings of switch S1, repeat steps (1) to (3).

(5) When Table D-2 is filled in, program the new decode PROM (74S287) using the addresses on the left side of the table and the data on the right side of the table. Unused addresses must be programmed to all zeroes.

TABLE D-2. ADDRESS-INPUT/DATA-OUTPUT OF ADDRESS DECODE PROM

Memory	Decode EPROM Address Input								Decode EPROM Output			
	MSB Address Lines					Switch S1 Setting						
	A0 ADH	A1 ADG	A2 ADF	A3 ADE	P10 ADD	S1/3 ADC	S1/2 ADB	S1/1 ADA	D04	D03	D02	D01
E1	—	—	—	—	—				1	0	0	1
E2	—	—	—	—	—	0 (ON)	0 (ON)	0 (ON)	1	0	1	0
RAM	—	—	—	—	—				1	1	0	0
E1	—	—	—	—	—				1	0	0	1
E2	—	—	—	—	—	0	0	1	1	0	1	0
RAM	—	—	—	—	—				1	1	0	0
E1	—	—	—	—	—				1	0	0	1
E2	—	—	—	—	—	0	1	0	1	0	1	0
RAM	—	—	—	—	—				1	1	0	0
E1	—	—	—	—	—				1	0	0	1
E2	—	—	—	—	—	0	1	1	1	0	1	0
RAM	—	—	—	—	—				1	1	0	0
E1	—	—	—	—	—				1	0	0	1
E2	—	—	—	—	—	1	0	0	1	0	1	0
RAM	—	—	—	—	—				1	1	0	0
E1	—	—	—	—	—				1	0	0	1
E2	—	—	—	—	—	1	0	1	1	0	1	0
RAM	—	—	—	—	—				1	1	0	0
E1	—	—	—	—	—				1	0	0	1
E2	—	—	—	—	—	1	1	0	1	0	1	0
RAM	—	—	—	—	—				1	1	0	0
E1	—	—	—	—	—				1	0	0	1
E2	—	—	—	—	—	1 (OFF)	1 (OFF)	1 (OFF)	1	0	1	0
RAM	—	—	—	—	—				1	1	0	0

NOTES: (1) E1 = EPROM Block 1, E2 = EPROM Block 2 (not used with TMS 2508's).
(2) Address line A3 must be a zero for TMS 2532's.
(3) At switch S1, an ON presents a zero to the decode PROM, and a OFF presents a one to the decode PROM.

D.5 EXAMPLES

D.5.1 Example 1

Figure D-2 is an example of programming the decode PROM for an EPROM of TMS 2508's, pin 10 of U25 wired to +5 V, and the following configurations of switch S1:

- S1 = ON ON ON
  EPROM at 0000
  RAM at F000
- S1 = ON ON OFF
  EPROM at 1000
  RAM at F000
- S1 = ON OFF ON
  EPROM at 2000
  RAM at F000

- S1 = ON OFF OFF
  EPROM at 3000
  RAM at F000
- S1 = OFF ON ON
  EPROM at 4000
  RAM at F000
- S1 = OFF ON OFF
  EPROM at 5000
  RAM at F000
- S1 = OFF OFF ON
  EPROM at 6000
  RAM at F000
- S1 = OFF OFF OFF
  EPROM at 7000
  RAM at F000

This will require the PROM to be programmed as follows:

PROM Address		Address Contents (Binary)
Binary	Hex	
0000 1000	08	1001
0001 1001	19	1001
0010 1010	2A	1001
0011 1011	3B	1001
0100 1100	4C	1001
0101 1101	5D	1001
0110 1110	6E	1001
0111 1111	7F	1001
1111 1000	F8	1100
1111 1001	F9	1100
1111 1010	FA	1100
1111 1011	FB	1100
1111 1100	FC	1100
1111 1101	FD	1100
1111 1110	FE	1100
1111 1111	FF	1100

All other addresses in the PROM must be programmed to all zeroes.

D.5.2 Example 2

Figure D-3 is an example of programming a decode PROM for using TMS 2516's with pin 10 of U25 wired to +5 V, and the following configurations of switch S1:

- S1 = ON ON ON
  EPROM Block 1 at E000
  EPROM Block 2 at F000
  RAM at 0000
- S1 = OFF OFF OFF
  EPROM Block 1 at 0000
  EPROM Block 2 at 1000
  RAM at F000

Memory	Decode EPROM Address Input								Decode EPROM Output			
	MSB Address Lines					Switch S1 Setting						
	A0 ADH	A1 ADG	A2 ADF	A3 ADE	P10 ADD	S1/3 ADC	S1/2 ADB	S1/1 ADA	D04	D03	D02	D01
E1	0	0	0	0	1				1	0	0	1
E2						0 (ON)	0 (ON)	0 (ON)	1	0	1	0
RAM	1	1	1	1	1				1	1	0	0
E1	0	0	0	1	1				1	0	0	1
E2						0	0	1	1	0	1	0
RAM	1	1	1	1	1				1	1	0	0
E1	0	0	1	0	1				1	0	0	1
E2						0	1	0	1	0	1	0
RAM	1	1	1	1	1				1	1	0	0
E1	0	0	1	1	1				1	0	0	1
E2						0	1	1	1	0	1	0
RAM	1	1	1	1	1				1	1	0	0
E1	0	1	0	0	1				1	0	0	1
E2						1	0	0	1	0	1	0
RAM	1	1	1	1	1				1	1	0	0
E1	0	1	0	1	1				1	0	0	1
E2						1	0	1	1	0	1	0
RAM	1	1	1	1	1				1	1	0	0
E1	0	1	1	0	1				1	0	0	1
E2						1	1	0	1	0	1	0
RAM	1	1	1	1	1				1	1	0	0
E1	0	1	1	1	1				1	0	0	1
E2						1 (OFF)	1 (OFF)	1 (OFF)	1	0	1	0
RAM	1	1	1	1	1				1	1	0	0

NOTE: E1 = EPROM Block 1, E2 = EPROM Block 2 (not used with TMS 2508's)

Figure D-2. Table Entries for Example 1

This will require the PROM to be programmed as follows:

PROM Address		Address Contents (Binary)
Binary	Hex	
1110 1000	78	1001
1111 1000	F8	1010
0000 1000	08	1100
0000 1111	0F	1001
0001 1111	8F	1010
1111 1111	FF	1100

All other addresses in the PROM must be programmed to all zeroes.

Memory	Decode EPROM Address Input								Decode EPROM Output			
	MSB Address Lines					Switch S1 Setting						
	A0 ADH	A1 ADG	A2 ADF	A3 ADE	P10 ADD	S1/3 ADC	S1/2 ADB	S1/1 ADA	D04	D03	D02	D01
E1	1	1	1	0	1				1	0	0	1
E2	1	1	1	1	1	0 (ON)	0 (ON)	0 (ON)	1	0	1	0
RAM	0	0	0	0	1				1	1	0	0
E1	—	—	—	—	—				1	0	0	1
E2	—	—	—	—	—	0	0	1	1	0	1	0
RAM	—	—	—	—	—				1	1	0	0
E1	—	—	—	—	—				1	0	0	1
E2	—	—	—	—	—	0	1	0	1	0	1	0
RAM	—	—	—	—	—				1	1	0	0
E1	—	—	—	—	—				1	0	0	1
E2	—	—	—	—	—	0	1	1	1	0	1	0
RAM	—	—	—	—	—				1	1	0	0
E1	—	—	—	—	—				1	0	0	1
E2	—	—	—	—	—	1	0	0	1	0	1	0
RAM	—	—	—	—	—				1	1	0	0
E1	—	—	—	—	—				1	0	0	1
E2	—	—	—	—	—	1	0	1	1	0	1	0
RAM	—	—	—	—	—				1	1	0	0
E1	—	—	—	—	—				1	0	0	1
E2	—	—	—	—	—	1	1	0	1	0	1	0
RAM	—	—	—	—	—				1	1	0	0
E1	0	0	0	0	1				1	0	0	1
E2	0	0	0	1	1	1 (OFF)	1 (OFF)	1 (OFF)	1	0	1	0
RAM	1	1	1	1	1				1	1	0	0

NOTE: E1 = EPROM Block 1, E2 = EPROM Block 2 (not used with TMS 2508's)

Figure D-3. Table Entries for Example 2

FACTORY REPAIR AND EXCHANGE POLICY

I. GENERAL

This policy specifies the conditions upon which a TM 990 product may be returned for repair subject to the terms of TI's warranty for such product.

WHEN A PRODUCT IS DEEMED ACCEPTABLE FOR REPAIR BY TI AND NO REQUEST HAS BEEN MADE FOR THE RETURN OF THE SAME SERIAL NUMBERED PRODUCT, TI RESERVES THE OPTION TO REPAIR OR EXCHANGE THE PRODUCT.

EPROMS CONTAINING CUSTOMER GENERATED SOFTWARE SHOULD BE REMOVED FROM A PRODUCT PRIOR TO SHIPMENT TO TI. THE REPLACEMENT BOARD MINUS SUCH EPROMS WILL THEN BE SHIPPED TO THE CUSTOMER. TI ACCEPTS NO RESPONSIBILITY FOR CUSTOMER GENERATED SOFTWARE SENT IN ON A UNIT TO BE REPAIRED.

II. NORMAL WARRANTY EXCHANGE OR REPAIR

Repair or exchange will be made free-of-charge provided:

i. The customer notifies TI of product failure within the applicable warranty period (90 days from the date of purchase from TI or from a TI authorized distributor) and

ii. TI's inspection discloses that the product is defective and that the defect is not the result of accident, misuse, neglect, alteration, improper installation, unauthorized repair or improper testing.

THE CUSTOMER SHALL BE RESPONSIBLE FOR PROVIDING PROOF OF THE DATE OF PURCHASE.

III. NON-WARRANTY EXCHANGE OR REPAIR

Non-warranty exchanges or repairs will be made for a charge in accordance with the schedule set forth in section VII below; provided such product is "repairable."

Product will be deemed "repairable" when the cost of repair does not exceed cost of replacement. If a product is not "repairable," the customer will be advised that repair cannot be effected and the product will be returned to the customer.

IV. SHIPPING INSTRUCTIONS

A. The following information must accompany the returned product. The TI Factory Repair and Exchange Questionnaire should be used to ensure that the required information is provided:

- Customer name and phone number
- Purchase order number (if applicable)
- Model number
- Serial number
- "Ship To" address; instructions for insurance and method of shipment (unless otherwise specified, TI will ship UPS, insured for the minimum)
- "Invoice To" address
- Description of symptoms of malfunction
- Type of service requested

(Note: The customer should retain a record of the model number and serial number identifying the returned product in the event that tracing of the product should be necessary.)

B. The product must be returned freight prepaid, F.O.B. TI's Factory Repair Center at:

Factory Repair Center
TM 990 Microcomputer Systems
Texas Instruments, Inc.
8500 Commerce Park Dr., Suite 110
Houston, TX 77036

C. Should the customer have any questions regarding this policy or the returned product status, he may contact the factory directly at: (713) 778-5729.

V. CUSTOMER CONFIGURATION

When the customer has made modifications to the product, repair or replacement will be "non-warranty."

TI will attempt the repair of such a product provided the customer has restored the product to its standard configuration. Labor and material will be charged at TI's then current standard rate for all necessary removals or repairs to customer-made modifications, if such is required to test the returned product in accordance with TI's specification for that product. TI reserves the right to refuse the repair of any product that has been modified such that the configuration as changed is untestable.

TI accepts no responsibility for additional memory, I/O terminator devices, or other devices added to a particular configuration and shipped on a product to be repaired.

VI. EXPEDITED SERVICE

Expedited service is available for an additional charge. It is available only on normal exchanges, subject to availability of replacement product confirmed by phone prior to shipment to TI. Replacement product will be shipped after receipt of the customer's defective product.

VII. CHARGES, TURNAROUND TIME AND METHOD OF PAYMENT

		Charge * (In Warranty)	Charge * (Non-Warranty)	Estimated Maximum Turnaround
1.	Normal exchange/repair	N/C	$150	10 normal working days
2.	Repair with customer configurations	N/A	$200	15 normal working days
3.	Expediting charge	$50	$50	48 hours

* Subject to change without notice. When the total estimated repair charge exceeds the standard charge such repair must have the prior written approval of the customer.

The customer must send payment, either in the form of a money order or check (company, cashier, or certified) with the product unless a purchase order is submitted. Payment must be made payable to Texas Instruments.

Product returns from the repair facility shall be made FOB TI factory. Transportation and insurance charges (if applicable) will be added on the invoice.

TI will invoice the customer on the date TI returns the repaired or exchanged product to the customer.

VIII. WARRANTY

Repaired or exchanged assemblies may contain either new parts or refurbished parts of like quality and are warranted to be free of defects in material and workmanship for a period of 30 days from date of shipment, provided such warranty repair shall not operate to reduce the original product warranty.

THE FOREGOING WARRANTIES FOR GOODS ARE IN LIEU OF ALL WARRANTIES, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO, ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE AND OF ANY OTHER WARRANTY OBLIGATION ON THE PART OF TI.

TM 990 MICROCOMPUTER SYSTEMS
TI Factory Repair and Exchange Questionnaire
(Please complete one questionnaire per product submitted)

SHIP TO			SOLD TO		
NAME/COMPANY			NAME/COMPANY		
ADDRESS-LINE 1			ADDRESS-LINE 1		
ADDRESS-LINE 2			ADDRESS-LINE 2		
CITY	STATE	ZIP	CITY	STATE	ZIP
USER NAME			USER PHONE NO. ( ) -		

(CHECK ONE) ☐ WARRANTY ☐ NON-WARRANTY	IF IN WARRANTY, IS PROOF OF PURCHASE DATE ENCLOSED? (CHECK ONE) ☐ YES ☐ NO

CHECK TYPE OF SERVICE REQUESTED	CUSTOMER P.O. NO.	AMT. OF PREPAID ($)
☐ NORMAL EXCHANGE/REPAIR ☐ REPAIR WITH CUSTOMER CONFIGURATIONS ☐ EXPEDITE	MODEL NO. TM 990/	SERIAL NO.
RETURN SHIPPING-PACKING INSTRUCTIONS*	INSURED? (CHECK ONE)* ☐ YES ☐ NO	LEVEL OF INSURANCE($)*

DESCRIPTION OF MALFUNCTION

BELOW FOR FACTORY USE ONLY

ORDER REC'D DATE	SUFFICIENT PAYMENT	R/E	FRN	ORDER SHIP DATE	

* Unless otherwise specified, TI will ship UPS, insured for the minimum.

Please save this portion and return
it with your product should
repair be necessary.

Use this form if the form attached
to the warranty card is lost.

TM 990/302 MICROCOMPUTER
USER RESPONSE SHEET

It is our desire to provide our customers with the best documentation possible. After using this manual, please complete this sheet and mail it, postpaid, to us. Your comments will be given every consideration.

1. Is the manual well organized? Yes_____ No_____ Comments:_____

2. Is text clearly presented and adequately illustrated? Yes_____ No_____

Comments: _____

3. What subject matter could be expanded or clarified? _____

4. Is the memory mapping adequately covered? Yes_____ No_____

Comments: _____

5. Are the interconnections and operation of the recorder/players adequately covered? Yes_____ No_____

Comments: _____

6. Please explain the application intended for your board:

School Course _____ Home _____ Evaluation _____ Other _____

7. Other comments concerning the TM 990/302 and this manual: _____

_____

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Name: _____

Address _____ State _____ ZIP _____

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