TEXAS INSTRUMENTS

TM 990

MICROPROCESSOR SERIES™

MANUAL HISTORY

This edition contains the following revisions:

Date	Revision Change (From - to)	ECN Number
3/03/83	D to E	461913

IMPORTANT NOTICES

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PREFACE

This document describes two Texas Instruments memory expansion boards: the TM 990/201 EPROM/RAM expansion board and the TM 990/206 RAM-only expansion board. Essentially, the TM 990/206 board is the TM 990/201 board with only the latter board's RAM circuitry and without its EPROM circuitry. The RAM circuitry is the same for both boards. The TM 990/201 is presented in detail in Sections 1 to 4, and the differences between the TM 990/201 and TM 990/206 are described in Section 5.

TMEM 2008 MEMORY EXPANSION MODULE

FEATURES

The TMEM 2008 memory expansion module has the following features:

- operates on the TM 990/103 microcomputer.
- provides an additional 16K of SRAM (through eight 20-pin sockets) to allow Main Memory expansion.
- connects to the host board via two 28-pin sockets and one 14-position header (J1).

SPECIFICATIONS

The TMEM 2008 has a temperature range of 0 to 70o C with forced air cooling of at least 100 linear feet per minute. The module requires a supply voltage of 5.0 Vdc $\pm$ 5%. The TMEM 2008-1 module has a 55 ns RAM access time.

The 20-pin sockets are populated with'4K x 4 high performance static RAMs.

The pinouts of the 14-pin header J1 are:

Pins	Signal	Pins	Signal
1-4	no connection	11	A3
5	CSC (selects U2, U4 data)	12	A4
6	CSD (selects U6, U8 data)	13	WE-
7-10	no connection	14	no connection

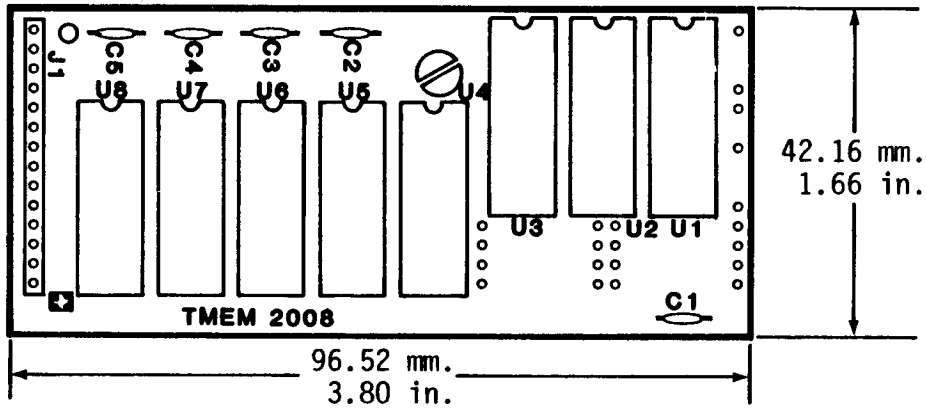

FIGURE 1. TMEM 2008 MEMORY EXPANSION MODULE

INSTALLATION PROCEDURE FOR THE TMEM 2008 MODULE

1. Turn off the power supply connected to the TM 990/103 microcomputer.
2. To expand Main Memory, remove the chips installed in sockets U43 and U51 and also remove the PAL in U19 and store them for future use; they will need to be reinserted in the TM 990/103 board if the TMEM 2008 is removed. A separate PAL (labelled U19 2008/2204) which contains the memory map for the TMEM 2008 is provided. Insert the 2008/2004 PAL in U19. Set switch S2 to all ON. RAM memory will be contiguous from $A000_{16}$ to $FFFE_{16}$.

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SECTION 1

INTRODUCTION

1.1 GENERAL

Sections 1 to 4 present detailed information on the TM 990/201 EPROM/RAM memory expansion board. Section 5 covers the TM 990/206 RAM-only memory expansion board and how it differs form the TM 990/201 board. Information applicable to the RAM configurations in Sections 1 to 4 is applicable to the TM 990/206.

The Texas Instruments TM 990/201 is an expansion memory board (shown in Figure 1-1) for use with the TM 990/100MA or TM 990/101MA microcomputers. The TM 990/201-44 expansion memory board is designed for use with the TM 990/1481 microcomputer. Features for the TM 990/201 boards include:

- Up to 8K words of 2114 static RAM (1024 x 4 bits each)
- Up to 16K words of TMS 2716 EPROM (2048 x 8 bits each)
- TTL compatible interface
- 3 MHz operating capability (5 MHz for TM 990/201-44)

The TM 990/201 is available in four versions as shown in Table 1-1. Access to the board is through the edge connector which mates to the backplane of the TM 990/510A OEM chassis (or the equivalent). The TM 990/201 board is not compatible with the TM 990/180M board which operates with an 8-bit data bus.

On Model TM 990/201-41, sockets are provided for 4K words of static RAM and 8K words of EPROM; however, only 2K words of RAM and 4K words of EPROM are populated. The TM 990/201-42, -43, -44 boards are totally socketed for up to 8K words of RAM and 16K words of EPROM and are populated in accordance with Table 1-1. Information in parentheses in Table 1-1 refers to the name of the memory block populated at the factory. Figure 1-2 shows memory board dimensions (for the TM 990/201 and /206). The TM 990/206 product matrix is shown in section 5.1, Table 5-1.

TABLE 1-1. TM 990/201 PRODUCT MATRIX

Model	Sockets Provided		Sockets Populated		RAM Access Time
	RAM	EPROM	RAM	EPROM	
TM 990/201-41	4K x 16 (RBLK0-RBLK1)	8K x 16 (EBLK4-EBLK7)	2K x 16 (RBLK0)	4K x 16 (EBLK6,EBLK7)	450 ns
TM 990/201-42	8K x 16 (RBLK0-RBLK3)	16K x 16 (EBLK0-EBLK7)	4K x 16 (RBLK0-RBLK1)	8K x 16 (EBLK4-EBLK7)	450 ns
TM 990/201-43	8K x 16 (RBLK0-RBLK3)	16K x 16 (EBLK0-EBLK7)	8K x 16 (RBLK0-RBLK3)	16K x 16 (EBLK0-EBLK7)	450 ns
TM 990/201-44	8K x 16 (RBLK0-RBLK3)	16K x 16 (EBLK0-EBLK7)	8K x 16 (RBLK0-RBLK3)	-0-	200 ns

Note: Block nomenclature explained in Section 3.

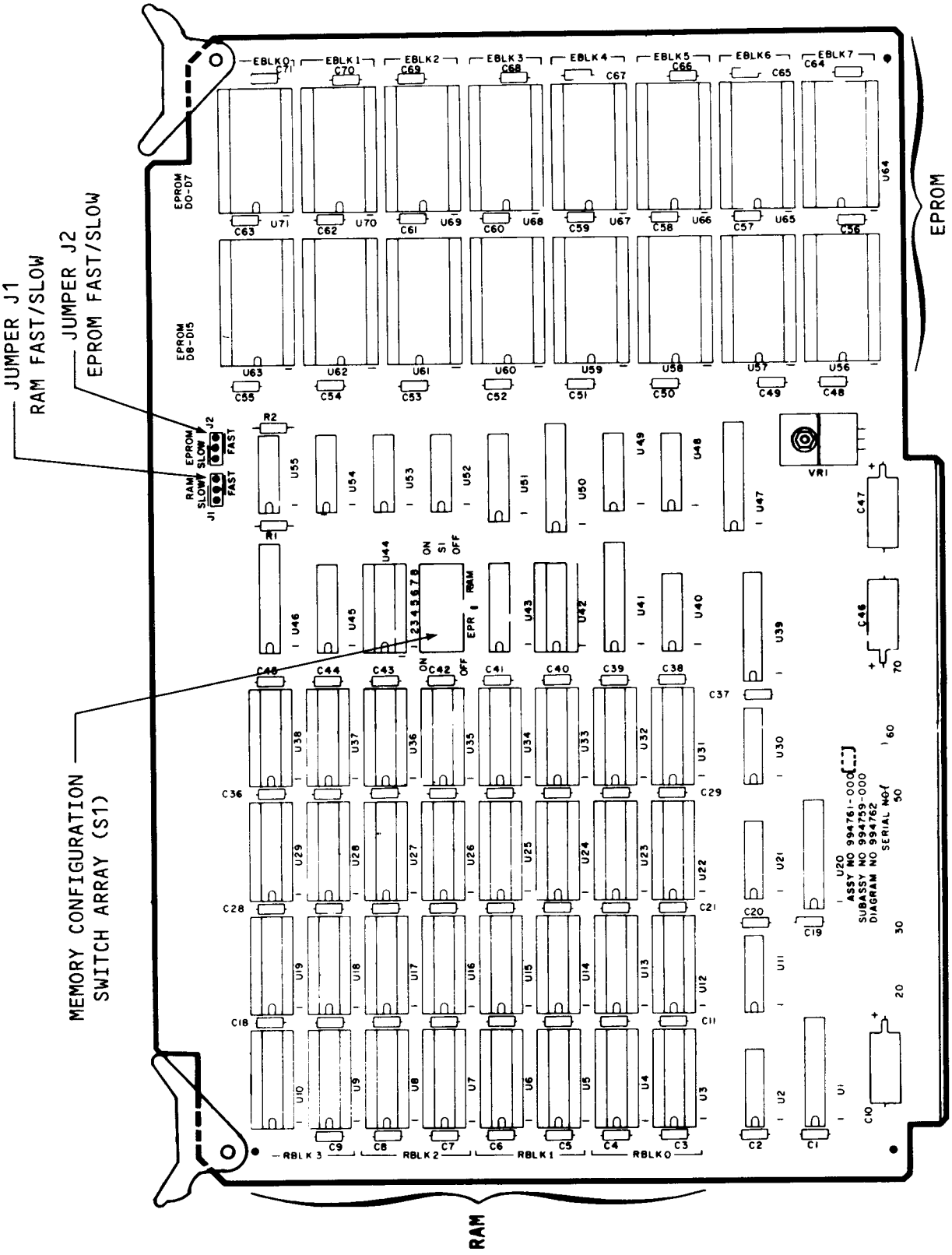


FIGURE 1-1. TM 990/201 MEMORY EXPANSION BOARD

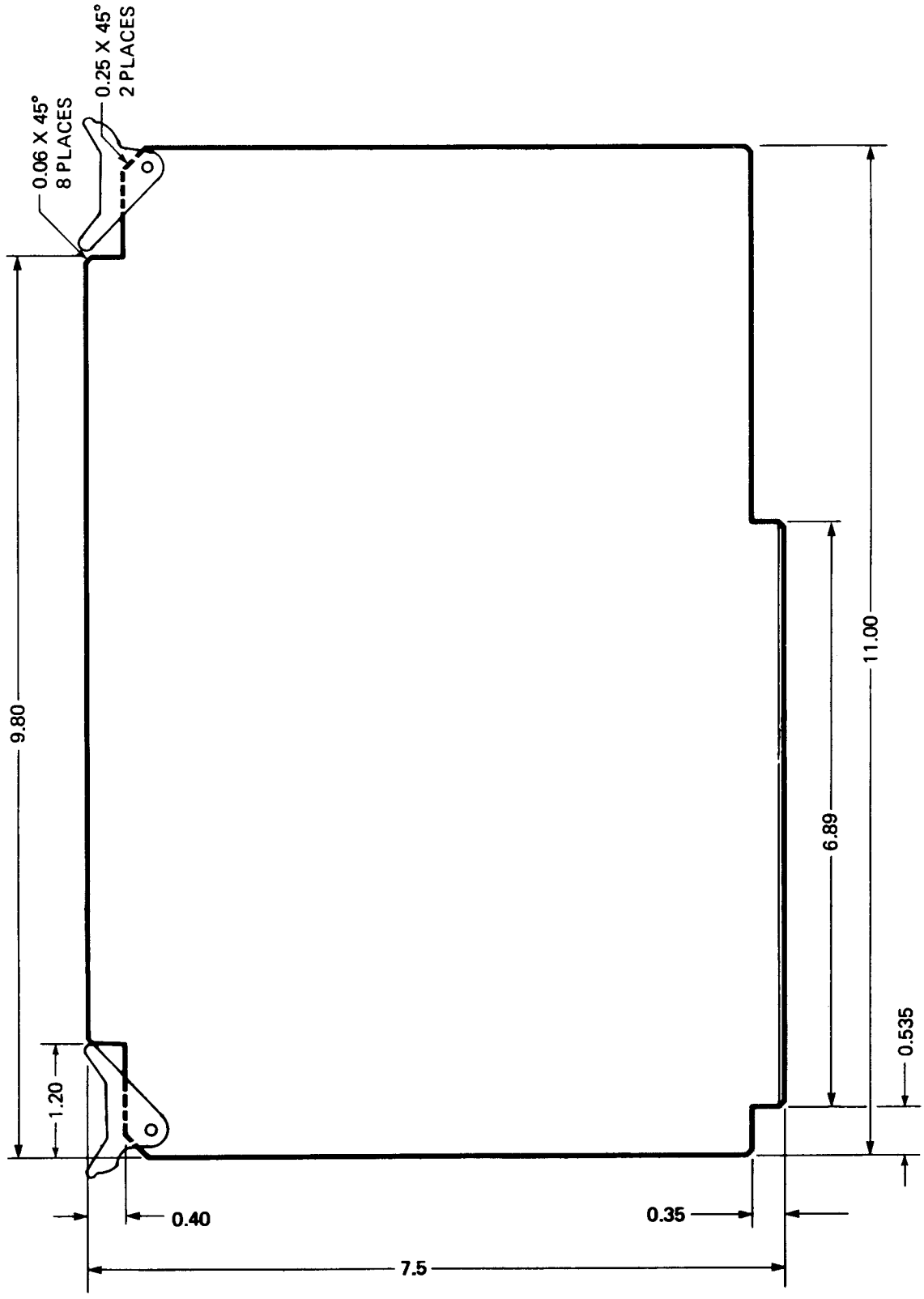


FIGURE 1-2. BOARD DIMENSIONS (IN INCHES)

1.2 MANUAL ORGANIZATION

Section 2 of this manual describes the correct procedure for installation, power-up, and operation of the TM 990/201 memory expansion board. Section 3 discusses memory mapping and operation of switch array S1 as well as jumpers J1 and J2. Section 4 discusses the theory of operation, including timing considerations and addressing. Section 5 outlines the differences between the TM 990/206 and the TM 990/201.

1.3 SPECIFICATIONS

Board Dimensions: See Figure 1-2.

Temperature Range: Operating 0°C to 70°C
Storage -40°C to 100°C

Clock rate: The TM 990/201 memory expansion board is compatible with the TM 990/100MA or TM 990/101MA CPU at 3 MHz. The TM 990/201-44 is compatible with the TM 990/1481 CPU at 5 MHz.

Devices Used: 2114 static RAM, 1K x 4
TMS 2716 EPROM, 2K x 8, 450 ns access time

Power: See Table 1-2.

1.4 APPLICABLE DOCUMENTS

- TM 990/100MA Microcomputer User's Guide
- TM 990/101MA Microcomputer User's Guide
- TM 990/1481 High-Performance CPU Module
- TMS 9900 Microprocessor Data Manual
- 74S481 Bit Slice Manual

TABLE 1-2. TM 990/201 POWER CONSUMPTION VS. SIZES

Model	Memory Size	+5V		+12V		-12V	
		Max	Typ	Max	Typ	Max	Typ
TM 990/201-41	2K RAM, 4K EPROM	2.5 A	1.0	.18 A	.16	.5 A	.05
TM 990/201-42	4K RAM, 8K EPROM	3.0 A	1.4	.38 A	.225	.55 A	.125
TM 990/201-43	8K RAM, 16K EPROM	5.5 A	2.15	.75 A	.475	.7 A	.225
TM 990/201-44	8K RAM, 16K EPROM	5.5 A	2.2	.75 A	.475	.7 A	.225

Note: Voltage tolerance ± 5% for all supplies.

SECTION 2

INSTALLATION AND OPERATION

2.1 GENERAL

This section explains the procedure for unpacking and setting up the TM 990/201 board for operation with a TM 990/100MA or TM 990/101MA microcomputer. The TM 990/201-44 can also be used with the TM 990/1481 microcomputer (see section 2.9.2 for set-up example).

2.2 REQUIRED EQUIPMENT

- TM 990/510A OEM chassis (or equivalent)
- Power supply that is capable of supplying the power requirements of the memory board (see Table 1-2), CPU, and other installed user equipment.
- Terminal
- TM 990/100MA or TM 990/101MA microcomputer (or TM 990/1481 microcomputer with fan cooled chassis)

2.3 UNPACKING

Take the TM 990/201 board from its carton and remove the protective wrapping. Check the board for any abnormalities that could have occured in shipping, and report any discrepancies to your supplier.

2.4 POWER AND TERMINAL HOOKUP

This procedure for hooking up a terminal and system power assumes a system of a TM 990/100MA, TM 990/101MA, or TM 990/1481 microcomputer, a TM 990/510A chassis, and a suitable terminal. (See the appropriate CPU User's Guide for description of proper terminals.) The power supply must provide all the necessary power requirements for the CPU board, the memory board, and any other boards the user may be using.

The use of a chassis is recommended because it offers protection from the abuse that a loose board would receive. It also provides termination resistors for the open collector signals used on the bus and allows system flexibility and hookup convenience.

There are two requirements that have to be met for proper operation of the TM 990/201: 1) proper selection of memory map and 2) proper hookup.

If the TM 990/510A chassis is used, the hookup is simple. Place the microcomputer in the first slot(s) of the chassis and place the memory board in the last slot. This positions the memory board between the CPU and the termination resistors on the backplane.

CAUTION

Always remove and insert boards with the power off. Do not insert or remove any board when the power is on as significant damage may result. If power is being supplied from separate power supplies, the system requires that -12 V be turned on first and be turned off last. There is no required sequence in turning on the remaining voltages. This does <u>not</u> apply if the system uses only one power supply.

2.5 MEMORY MAPPING

Care in selection of the memory map is important before powerup. Refer to Section 3 for details in memory placement and selection of address configuration using switch array S1.

2.6 MEMORY ACCESS SPEED

Jumpers J1 and J2 (Figure 1-1) must be set to FAST or SLOW to indicate respectively the access time of the RAM or EPROM memories used. Table 2-1 lists access time and J1/J2 settings. Section 4.8.1 explains these timing constraints in detail.

TABLE 2-1. MEMORY ACCESS TIME AND J1/J2 SETTINGS

Memory Access Time	J1 (RAM) and J2 (EPROM) Setting at Clock Rate 3 MHz	5 MHz
450 ns	SLOW	SLOW
300 ns	FAST	SLOW
200 ns	FAST	FAST
150 ns	FAST	FAST

2.7 BOARD ACCESS TIME

The maximum board access time for TM 990/201 is 486 ns. The only exception is the RAM access time for the TM 990/201-44 which is 236 ns.

2.8 OPERATION

Essentially the user needs only to choose the correct memory configuration (Section 3), insert the board into the chassis, and apply power to set-up the system for operation.

The operation of the TM 990/201 memory board should be transparent to the user in that no special signals are required other than those supplied through the backplane. If the TM 990/510A chassis (or equivalent) is not used, refer to section 4.10 for interface information.

2.9 EXAMPLES

2.9.1 Set-up with TM 990/100MA or TM 990/101MA Microcomputer

This example assumes the following configurations:

1) TM 990/100MA or TM 990/101MA microcomputer
   - 4K x 16 EPROM in memory address (M.A.) 0000_{16} to $1FFF_{16}$
   - 512 x 16 RAM in M.A. $FC00_{16}$ to $FFFF_{16}$

2) TM 990/201 expansion board
   - 4K x 16 EPROM
   - 2K x 16 RAM

Figure 2-1 depicts the desired memory map. Note that expansion EPROM resides at address 2000_{16} to $3FFF_{16}$ while expansion RAM on the TM 990/201-41 is to reside in locations $E000_{16}$ to $EFFF_{16}$ of the TM 990/100MA or TM 990/101MA address map.

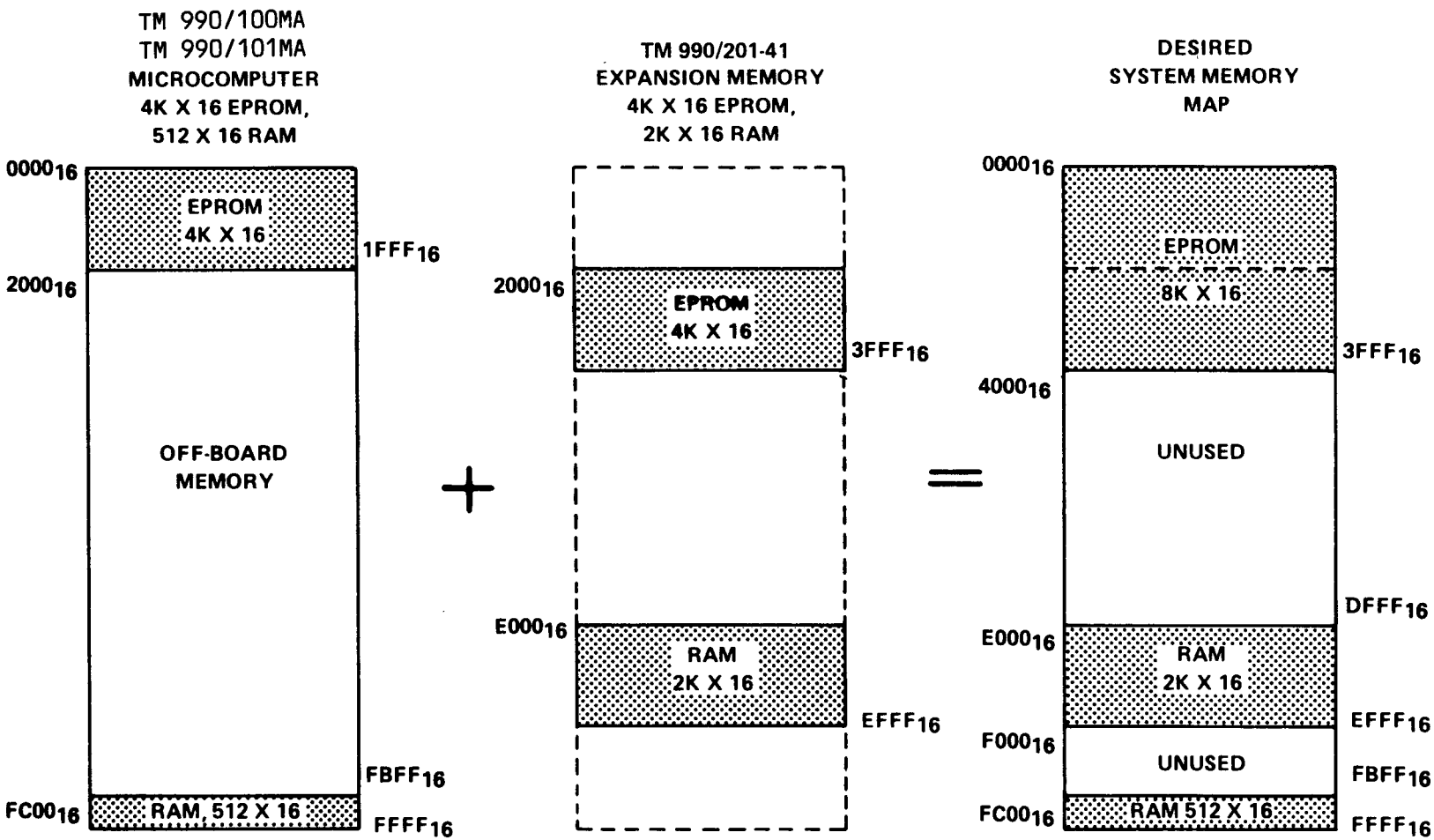


FIGURE 2-1. TM 990/201 MEMORY MAP EXAMPLE

The user must do four things to the TM 990/201-41 prior to interfacing the unit to the microcomputer:

1) Configure the expansion RAM into the TM 990/100MA or TM 990/101MA memory map using switch S1 and memory placement on the board.

2) Configure the expansion EPROM into the TM 990/100MA or TM 990/101MA memory map using switch S1 and memory placement on the board.

3) Select the wait state for RAM using jumper J1.

4) Select the wait state for EPROM using jumper J2.

2.9.1.1 Configure Memory Map

Populate the EPROM and RAM as explained in section 3.2.2 and Figure 3-6.

To map EPROM into the desired address bounds, set the memory configuration switch array (S1) to ON-ON-OFF-OFF as shown in Figure 3-2 (switches 1 to 4).

To map RAM into the desired address bounds, set switch array S1 to OFF-ON-OFF-OFF as shown in Figure 3-4 (switches 5 to 8).

Section 3 explains memory placement, mapping, and selection of S1 switches.

2.9.1.2 Select Wait State

The TM 990/100MA or TM 990/101MA operates at 3 MHz. The TM 990/201-41 is shipped with 2114 RAM's, 450 nsec access time. Thus, place the RAM FAST/SLOW jumper (J1) in the "SLOW" position. The TM 990/201-41 is shipped with TMS 2716 EPROM's which have a 450 nsec access time. Place the EPROM FAST/SLOW jumper (J2) in the "SLOW" position.

The switch array and the FAST/SLOW jumpers are shown in Figure 1-1. Note that each switch of the array is numbered and each switch is designated as either "ON" (a zero) or "OFF" (a one). The FAST/SLOW jumper positions are also marked "FAST" or "SLOW".

2.9.2 Set-up with TM 990/1481 Microcomputer

This example assumes the following configurations:

1) TM 990/1481 microcomputer with no on-board memory

2) TM 990/201-44 expansion memory board
   - 16K x 16 EPROM
   - 8K x 16 RAM

Figure 2-2 shows a sample memory map achieved with the TM 990/201-44.

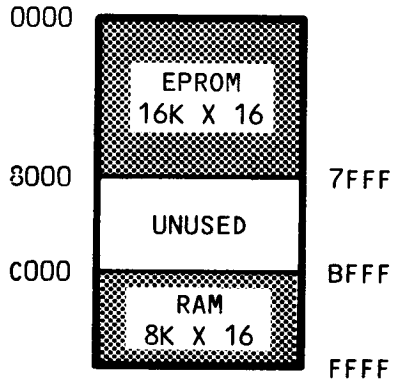


FIGURE 2-2. TM 990/201-44 MEMORY MAP EXAMPLE

The user must do four things to the TM 990/201-44 prior to interfacing the unit to the microcomputer.

- Configure the expansion RAM using switch S1
- Configure the expansion EPROM using switch S1
- Select the wait state for RAM using jumper J1
- Select the wait state for EPROM using jumper J2

2.9.2.1 Configure Memory Map

Populate EPROM and RAM as explained in section 3.2.2 and Figure 3-6.

To map EPROM into the desired address bounds as shown in Figure 2-2, set the memory switch array (S1) to ON-ON-ON-ON as shown in Figure 3-3 (switches 1 to 4).

To map RAM into the desired address bounds as shown in Figure 2-2, set the memory switch array (S1) to ON-OFF-OFF-OFF as shown in Figure 3-5 (switches 5 to 8).

Section 3 explains memory placement, mapping, and selection of S1 switches.

2.9.2.2 Select Wait State

TM 990/1481 operates at 5 MHz. The TM 990/201-44 is shipped with 2114 RAM's which have a 200 ns access time. Place the FAST/SLOW jumper (J1) in the "FAST" position. If TMS 2716 EPROMS with 450 ns access time are used, J2 should be in the "SLOW" position.

The switch array and the FAST/SLOW jumpers are shown in Figure 1-1. Note that each switch of the array is numbered and each switch position is designated as either "ON" (a zero) or "OFF" (a one). The FAST/SLOW jumper positions are marked "FAST" or "SLOW".

SECTION 3

MEMORY PLACEMENT AND SELECTION

3.1 GENERAL

This section describes the procedures used to map memory located on the TM 990/201 memory board into the available address space. Switch S1 and address decode PROM's U42 and U44 determine the address space occupied by both EPROM and RAM on the TM 990/201 board. To select a memory address configuration which is compatible with the system memory map, the user must first do the following:

1) Determine the quantity of EPROM and RAM to be populated on the board.

2) Place the EPROM and RAM devices in their correct physical locations on the board.

3) Set the memory configuration switch array (S1) so that the memory on the TM 990/201 board is mapped into an available address space unoccupied on another board in the system. This address space must be large enough to contain the amount of memory on the TM 990/201 board, and it must not conflict with the same addresses populated on another board.

CAUTION

If there are overlaying duplicate addresses on different boards in the configured system, the resulting data bus conflict may cause damage to the data bus drivers on these boards.

3.2 MEMORY PLACEMENT

Settings of memory configuration switch array (S1, center of the board, see Figure 1-1) determine the address configuration that will be decoded by the address decoding circuitry - two SN74S287 PROM's programmed at U42 for decode EPROM and U44 for decode RAM. Switch array S1 selects the memory starting address and the quantity of memory starting at that address.

3.2.1 Memory Configuration Switch Array (S1)

The memory configuration switch array is divided into two parts. The left four slide switches (1 to 4) designate the EPROM configuration. The right four slide switches (5 to 8) designate the RAM configuration. If the switch is set to the ON position, a binary "0" is encoded at the switch. If the switch is set in an OFF position, a binary "1" is encoded. These switch settings designate the four-bit codes that select the EPROM and RAM address configuration. Figure 3-1 shows the memory configuration switch array.

Note that when read right to left (4 to 1 and 8 to 5), the switches form the binary code 0_{16} to F_{16} as used at the top of Figures 3-2 to 3-5 to explain switch settings and memory addresses. Note again that OFF refers to a binary "1" and ON refers to a binary "0". As shown in Figures 3-2 to 3-5, switch array S1 selects the starting address and the quantity of memory decoded. For example, if switches 1 to 4 are set to all ON's, the memory decoder will select all 16 EPROM sockets (16K words) using addresses beginning at 0000_{16} (0000_{16} to $7FFF_{16}$). If switches 1 to 4 are set to OFF-ON-ON-ON respectively,

the memory decoder will decode all EPROM sockets populated using a starting address of 2000_{16} (2000_{16} to $9FFF_{16}$).

Also shown in Figures 3-2 and 3-3 are EPROM memory address configurations for 8K words and 4K words, all switch selectable.

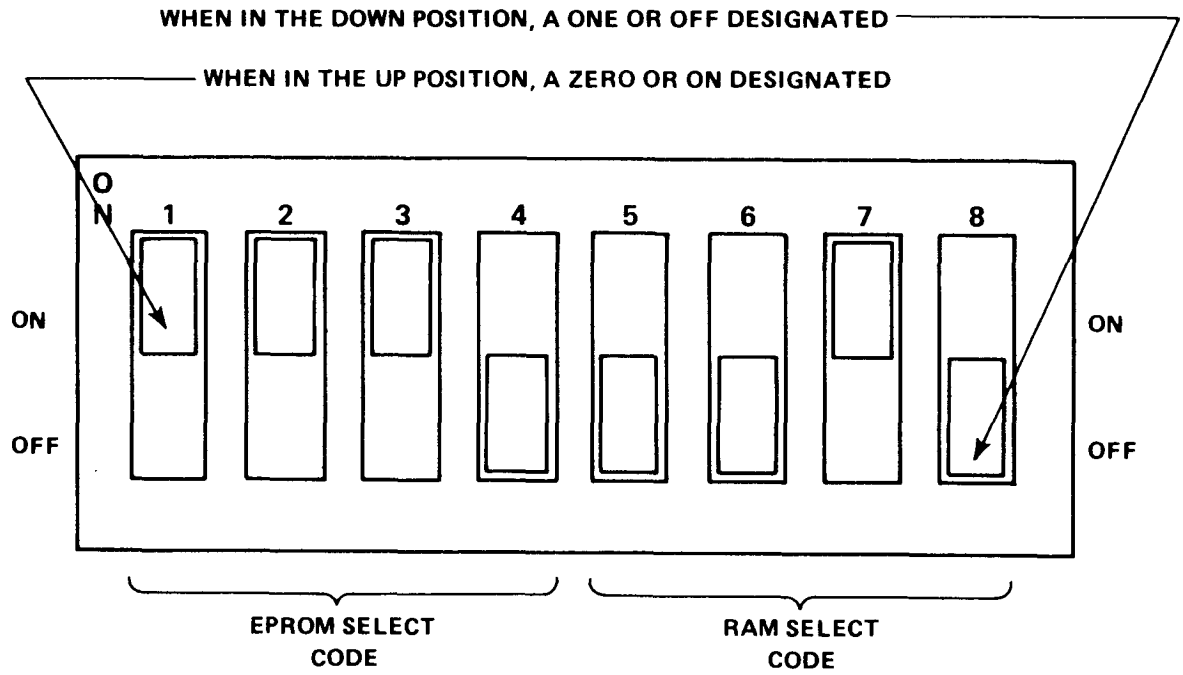
Switch decoding for RAM selection is shown in Figures 3-4 and 3-5. For example, if switches 5 to 8 are set to OFF-OFF-OFF-ON (Figure 3-4), the memory decoder will select 6K of RAM using addresses 0000_{16} to $2FFF_{16}$.

Not all EPROM's or RAM's populated on the board need be selected by switch S1. Memory not selected by the S1 setting will not be enabled although populated on the board. Conversely, if less memory is populated on the board than designated by switch array S1, the decode logic will address memory as if it was populated as shown by S1.

CAUTION

The user must exercise care in configuring the TM 990/201 memory into a system. The memory map of the TM 990/201 must not overlay memory on other boards in the system. The resulting data bus conflict may cause damage to data bus drivers on the TM 990/201 or other boards in the system. Note that Figures 3-2 and 3-4 contain blocks to show the memory configuration on the microcomputer board. Consider this memory when selecting expansion memory configurations.

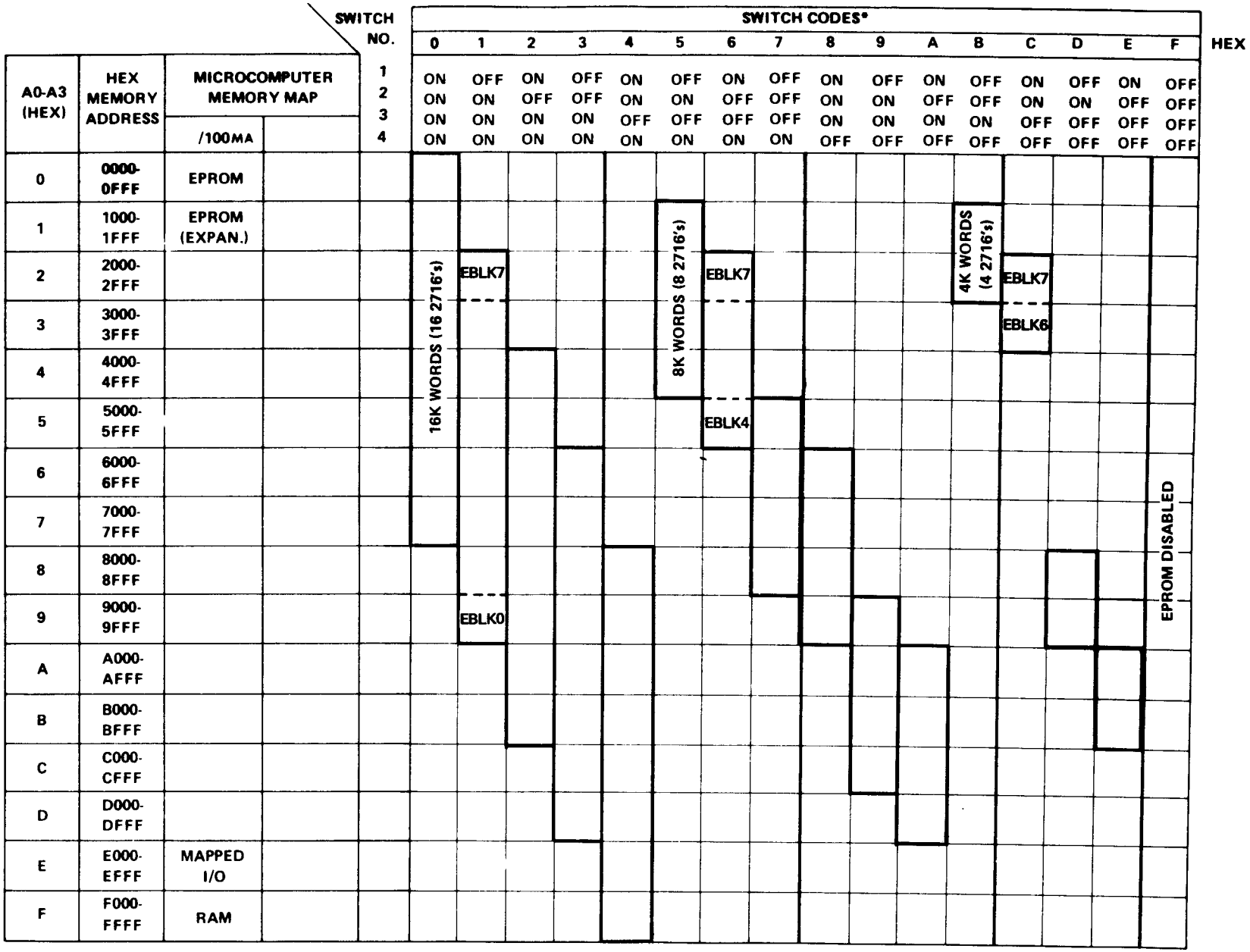
Figures 3-2 to 3-5 show that setting switches 1 to 4 or 5 to 8 to all OFF (OFF-OFF-OFF-OFF) will disable all EPROM or RAM.



NOTE: SWITCH SETTINGS FURTHER EXPLAINED IN FIGURES 3-2 (EPROM) AND 3-3 (RAM)

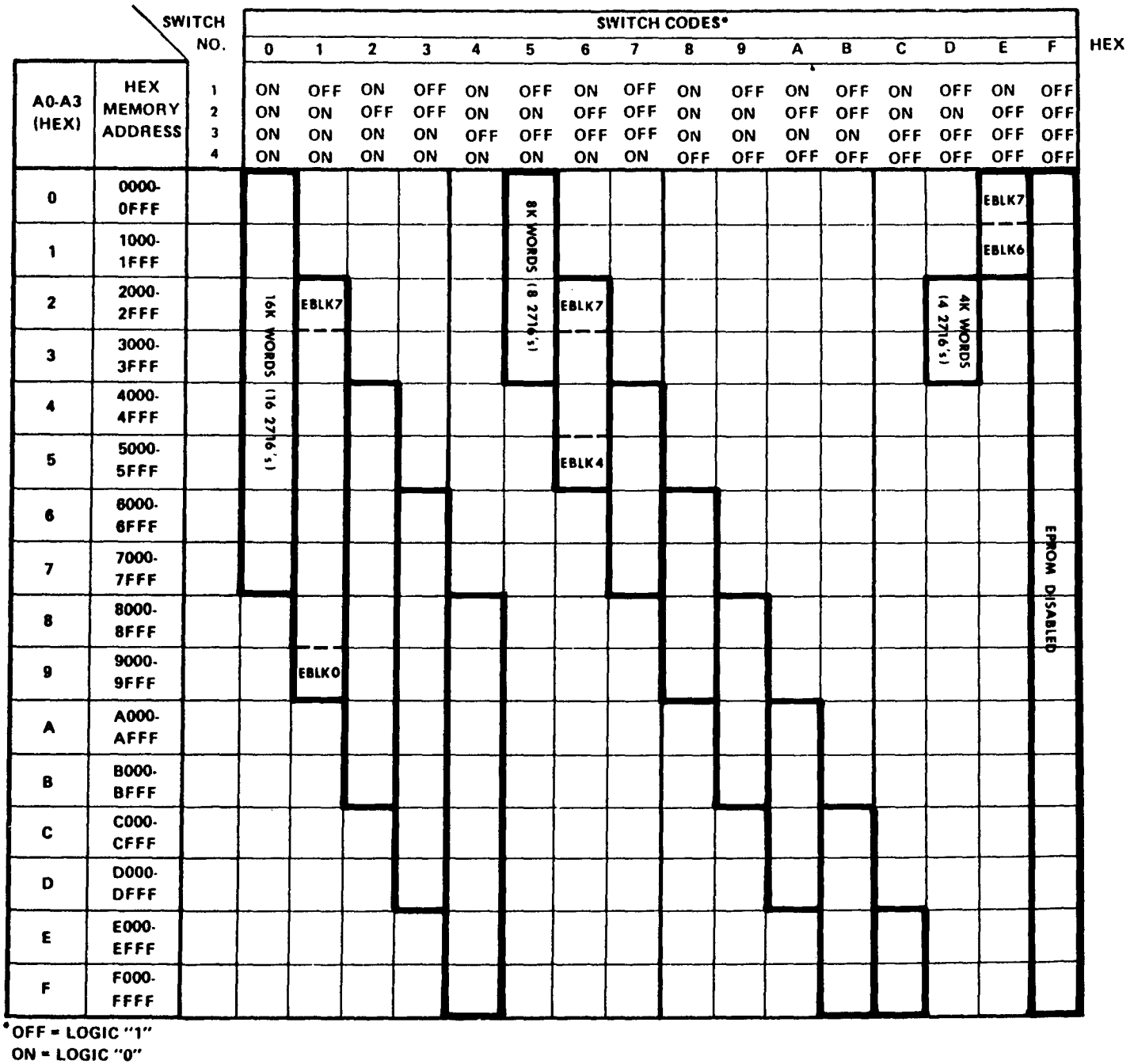
FIGURE 3-1. MEMORY CONFIGURATION SWITCH

Note: Switch settings are further explained in Figures 3-2, 3-3 (EPROM) and in Figures 3-4, 3-5 (RAM).



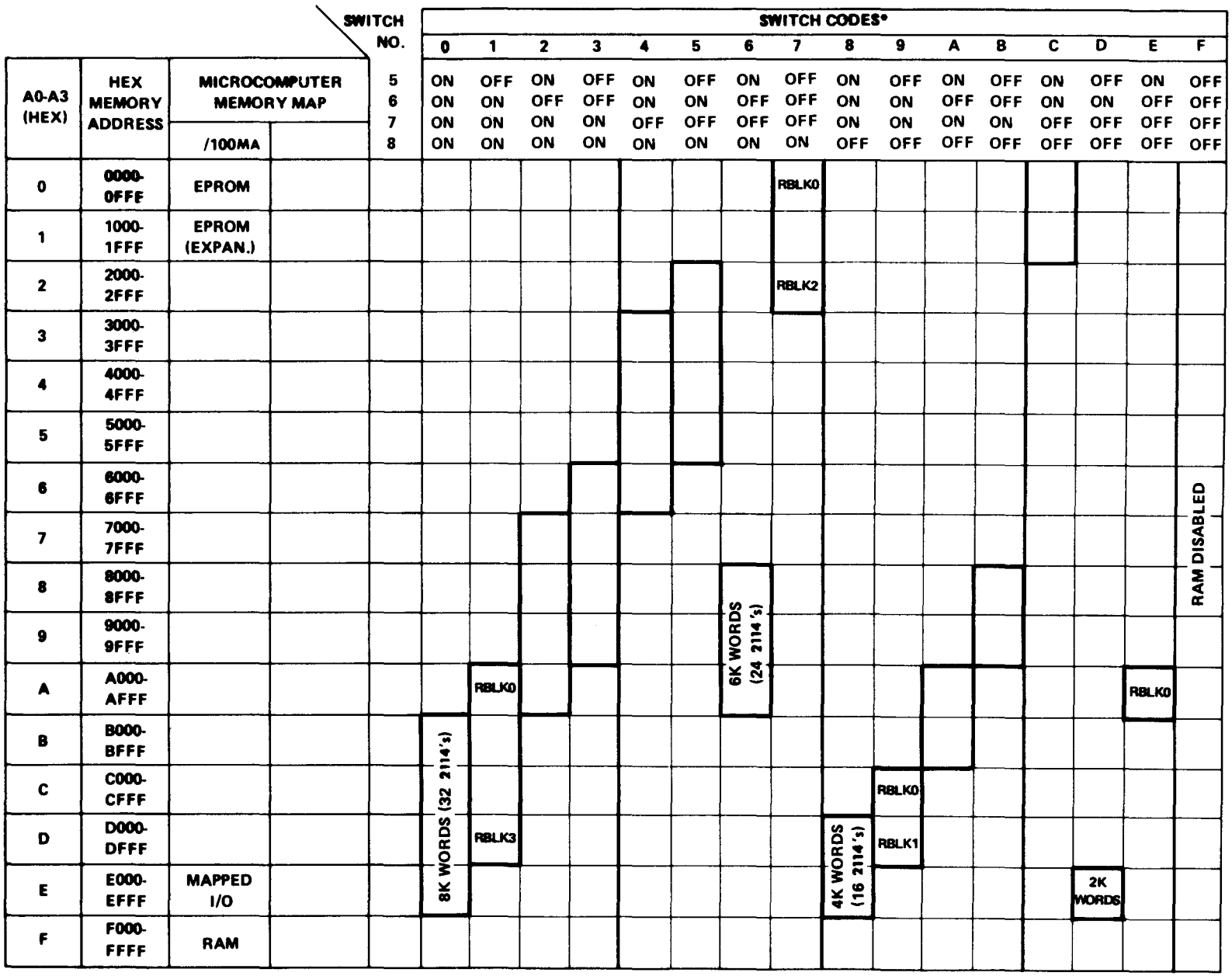
*OFF = binary "1"
ON = binary "0"

FIGURE 3-2. TM 990/201-41, -42, -43 EPROM MEMORY CONFIGURATIONS



*OFF = LOGIC "1"
ON = LOGIC "0"

FIGURE 3-3. TM 990/201-44 EPROM MEMORY CONFIGURATIONS



*OFF = 1, ON = 0

FIGURE 3-4. TM 990/201-41, -42. -43 RAM MEMORY CONFIGURATIONS

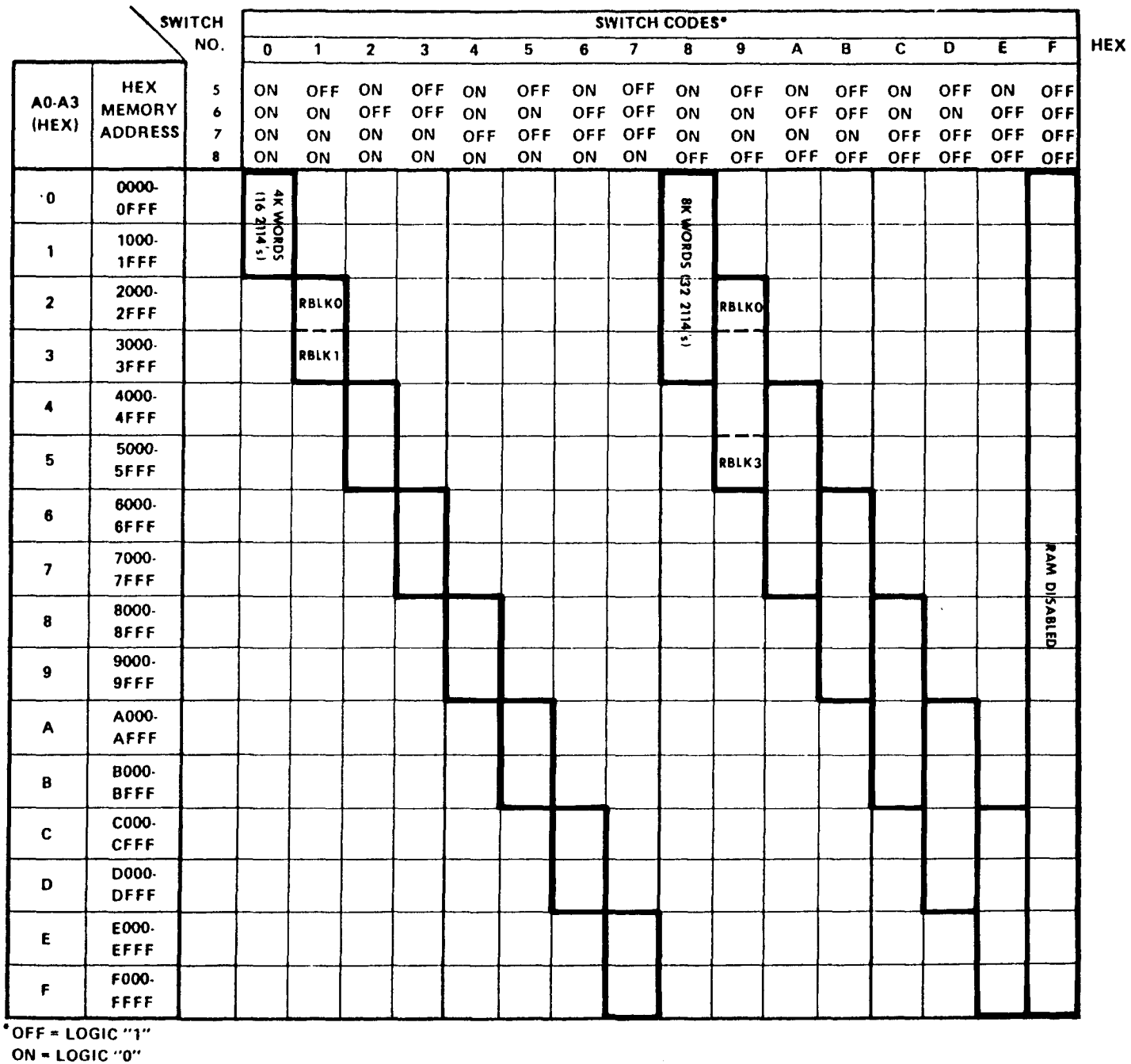


FIGURE 3-5. TM 990/201-44 RAM MEMORY CONFIGURATIONS

3.2.2 Memory Placement by Blocks

EPROM is organized into eight 2K-word blocks designated EBLK0 to EBLK7; RAM is organized into four 2K-word blocks designated RBLK0 to RBLK3 as shown in Figure 3-6.

Encoded as the beginning of onboard memory are EPROM block 7 (EBLK7) and RAM block 0 (RBLK0). In other words, memory decode logic will map memory from low to high in the following order of blocks.

EPROM	RAM
EBLK7 (lowest address)	RBLK0 (lowest address)
EBLK6	RBLK1
EBLK5	RBLK2
EBLK4	RBLK3 (highest address)
EBLK3	
EBLK2	
EBLK1	
EBLK0 (highest address)	

As shown in Figure 3-6, each block of RAM consists of two 4-chip rows of 2114's. Each row consists of 1K by 16-bits, with the bottom row at the lower addresses and the upper row at the higher addresses.

3.2.2.1 EPROM Examples

If the memory configuration switch is set to a code of OFF-ON-OFF-ON (Figure 3-2), indicating 8K words of EPROM, the following will be mapped by the memory decode logic:

BLOCK	MEMORY ADDRESS
EBLK7	1000_{16} to $1FFF_{16}$
EBLK6	2000_{16} to $2FFF_{16}$
EBLK5	3000_{16} to $3FFF_{16}$
EBLK4	4000_{16} to $4FFF_{16}$

NOTE

Even though other EPROM blocks may be populated, only those denoted in Figure 3-2 will be selected for a given setting of switch S1.

If the memory configuration switch is set to a code of OFF-ON-OFF-OFF (Figure 3-2), indicating 4K of EPROM, the following will be mapped by the memory decode logic:

BLOCK	MEMORY ADDRESS
EBLK7	8000_{16} to $8FFF_{16}$
EBLK6	9000_{16} to $9FFF_{16}$

3.2.2.2 RAM Example

If the memory configuration switch is set to a code of OFF-OFF-OFF-ON (Figure 3-4), the following will be mapped by the memory decode logic:

BLOCK	MEMORY ADDRESS
RBLK0	0000_{16} to $0FFF_{16}$
RBLK1	1000_{16} to $1FFF_{16}$
RBLK2	2000_{16} to $2FFF_{16}$

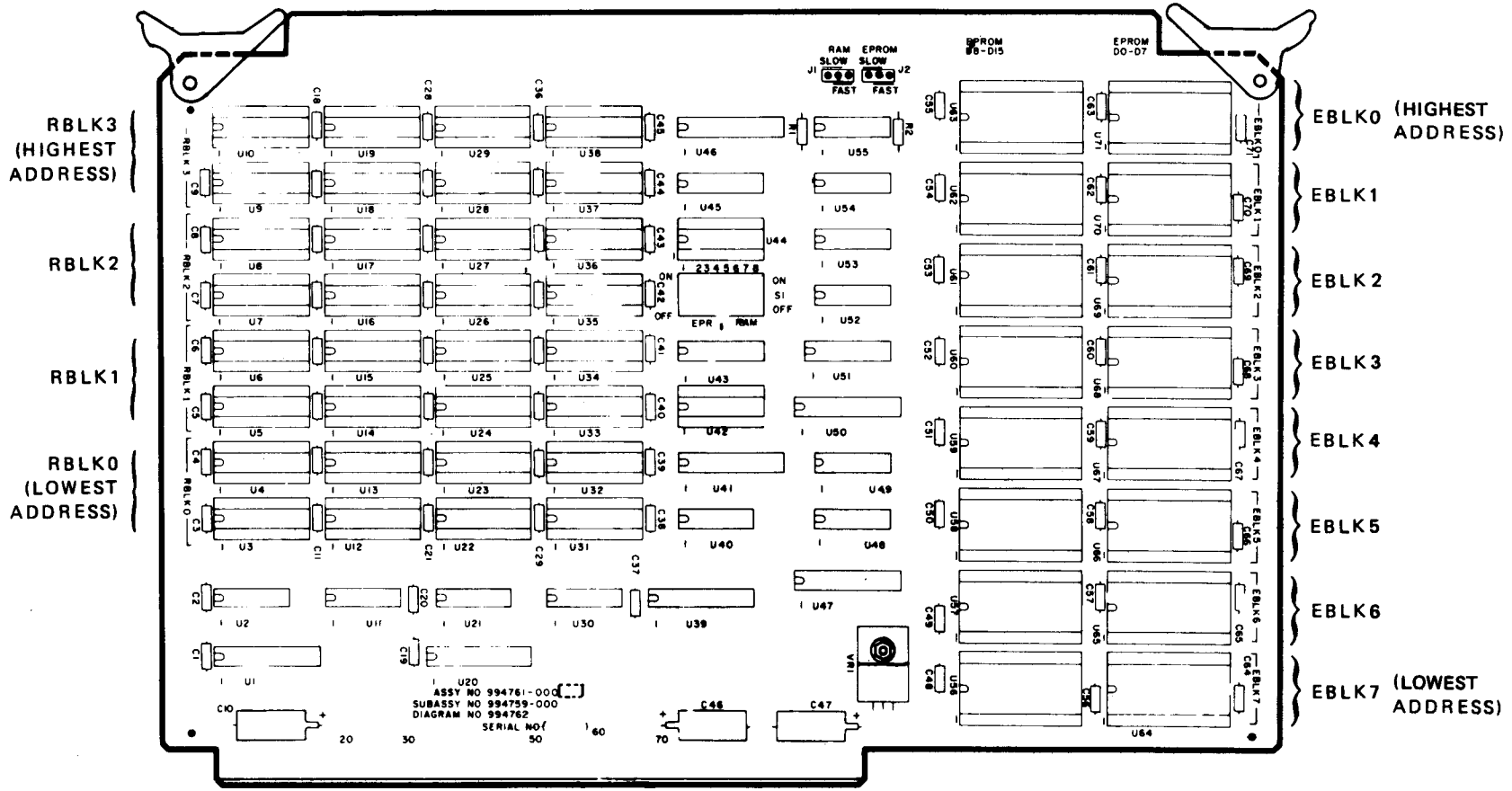


FIGURE 3-6. MEMORY BLOCK LOCATIONS

SECTION 4

THEORY OF OPERATION

4.1 GENERAL

This section covers the theory of operation of the TM 990/201. Information in the TMS 9900 Microprocessor Data Manual can supplement the material in this section. Figure 4-1 is a block diagram of the TM 990/201 memory board. Figure 1-1 is a picture of the TM 990/201 detailing the position of its primary components.

4.2 STATIC RAM SECTION

The static RAM section of the TM 990/201 expansion memory board uses 2114, 1K x 4-bit static RAM. Table 1-1 defines the product matrix and the amount of RAM on each board. A fully populated TM 990/201 consists of four 2K x 16 blocks of RAM. These blocks are designated RBLK0, RBLK1, RBLK2, and RBLK3.

For the TM 990/201, RBLK0 always appears first in the RAM address space followed by RBLK1. RBLK3 is always the last 2K word block of RAM decoded. The block numbers are designated in silkscreen on the TM 990/201.

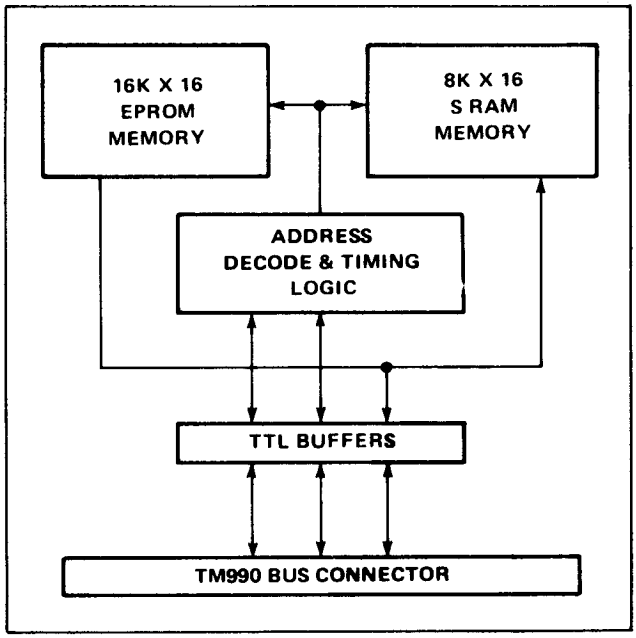


FIGURE 4-1. TM 990/201 BLOCK DIAGRAM

4.3 EPROM SECTION

The EPROM section of the TM 990/201 memory board uses TMS 2716, 2K x 8-bit EPROM. Table 1-1 defines the product matrix and the amount of EPROM on each board. A fully populated TM 990/201 consists of eight 2K x 16 blocks of EPROM. These are designated EBLK0 through EBLK7.

EBLK7 is always decoded first in the EPROM address space followed by EBLK6. EBLK0 always appears as the last 2K word block of memory on the TM 990/201. The block numbers are designated in the board's silkscreen.

4.4 ADDRESS MAP OPTIONS

The TM 990/201 can be configured in a variety of way into the address map of a TM 990/100MA or TM 990/101MA microcomputer system. The switch states of switch array S1, an 8-position DIP switch array, uniquely determine the mapping of the TM 990/201 EPROM and RAM memory arrays. Switches 1 through 4 select the mapping of the EPROM memory array. Switches 5 through 8 select the RAM mapping. Figure 4-2 summarizes in block diagram form the address decode logic. Selection of memory mapping using S1 is explained in Section 3.

The possible maps for the EPROM and RAM arrays are shown in Figures 3-2 to 3-5. As explained in Section 3, each switch code corresponds to a unique location of the EPROM or RAM in the memory address space. The switch code implies the starting address of the entire block of EPROM or RAM on the TM 990/201 and the amount of EPROM or RAM selected on the TM 990/201.

The EPROM decode logic maps the EPROM into a contiguous memory space. EPROM block 7 (designated EBLK7 in silkscreen) is mapped into the first 2K word block of this address space followed by block 6 and so on. Block 0 is the last block mapped. This is true of all EPROM mapping options. For code 5 (in Figure 3-2), EBLK7 is mapped into 1000_{16} to $1FFF_{16}$; EBLK6 into 2000_{16} to $2FFF_{16}$; EBLK5 into 3000_{16} to $3FFF_{16}$; and EBLK4 into 4000_{16} to $4FFF_{16}$. All other EPROM blocks are disabled for code 5 even if they are populated.

The RAM decode logic also maps the RAM array into a contiguous address space. RAM block 0 (RBLK0 designated in silkscreen) is always mapped into the first 2K words of the space. This is always followed by block 1 and so on. Block 3 is mapped into the last 2K word block.

The decode logic permits RAM precedence over EPROM if both RAM and EPROM are configured in the same address space. This feature is very convenient in debugging programs which will be ROM resident. They may be debugged in RAM on the TM 990/201. Once they are "clean," they may be programmed directly into EPROM without relocation and the attendant relinking.

4.5 EPROM DECODE LOGIC

Figure 4-3 depicts the EPROM decode logic. Switch positions 1 through 4 select a 16-"nibble" (4 bits, half a byte) block of memory in the 74S287. Each block corresponds to 1 of 12 possible EPROM address maps. Each nibble in the block determines:

1) If a block of EPROM is to be selected during the current memory cycle given the current state of address bits A0 to A3.

2) Which block of EPROM (EBLK7 through EBLK0) is selected.

The three least significant data bits from the 74S287 PROM (D01 to D03) select the block of EPROM. A state of 0 corresponds to EPROM block 0 while a state of 7 corresponds to EPROM block 7. The most significant bit (D04) enables the 1-of-8 selector along with the memory enable signal (MEMEN.M) from the microcomputer. The 1-of-8 selector (74LS138) develops the EPROM select signals.

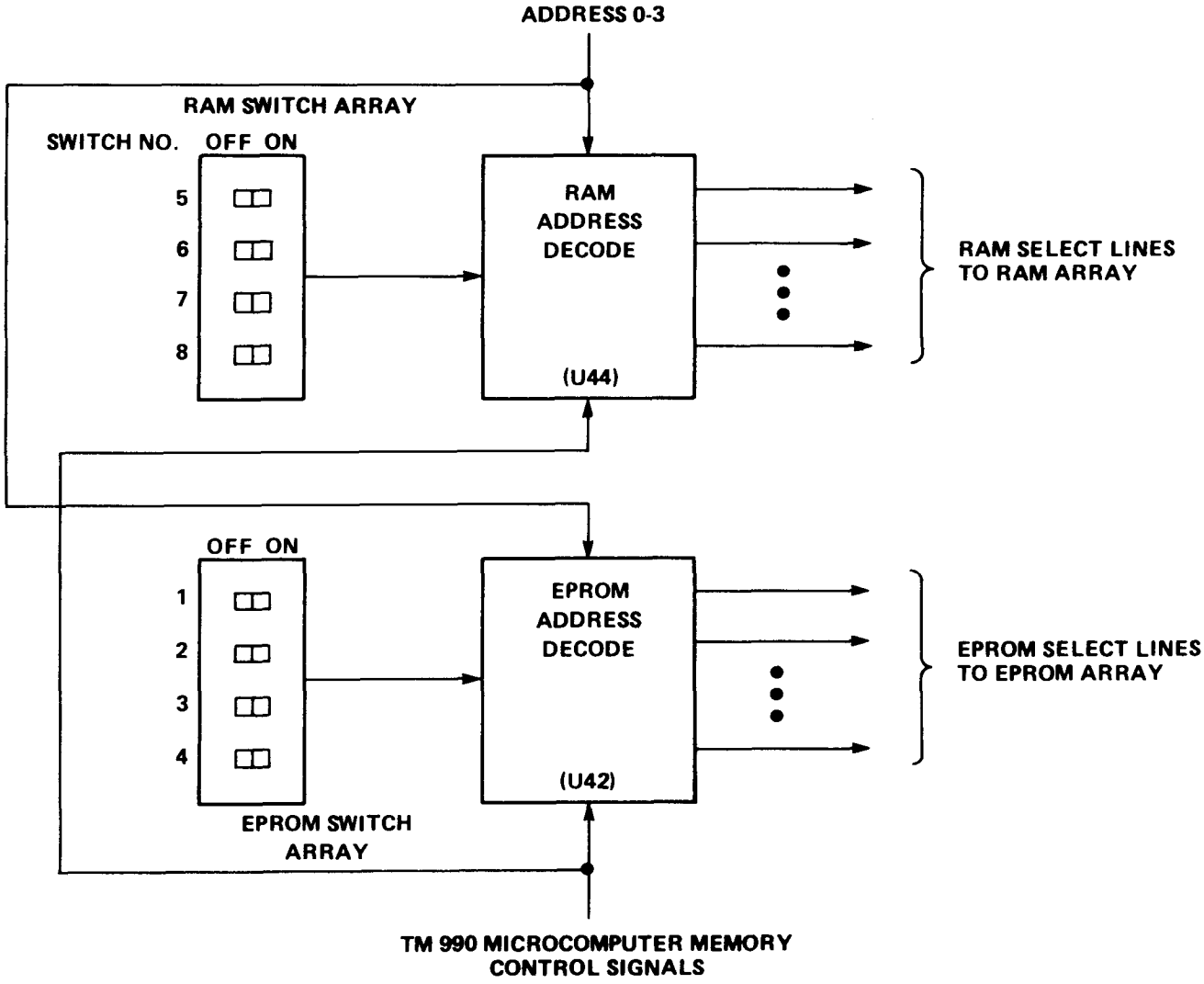


FIGURE 4-2. TM 990/201 ADDRESS DECODE LOGIC BLOCK DIAGRAM

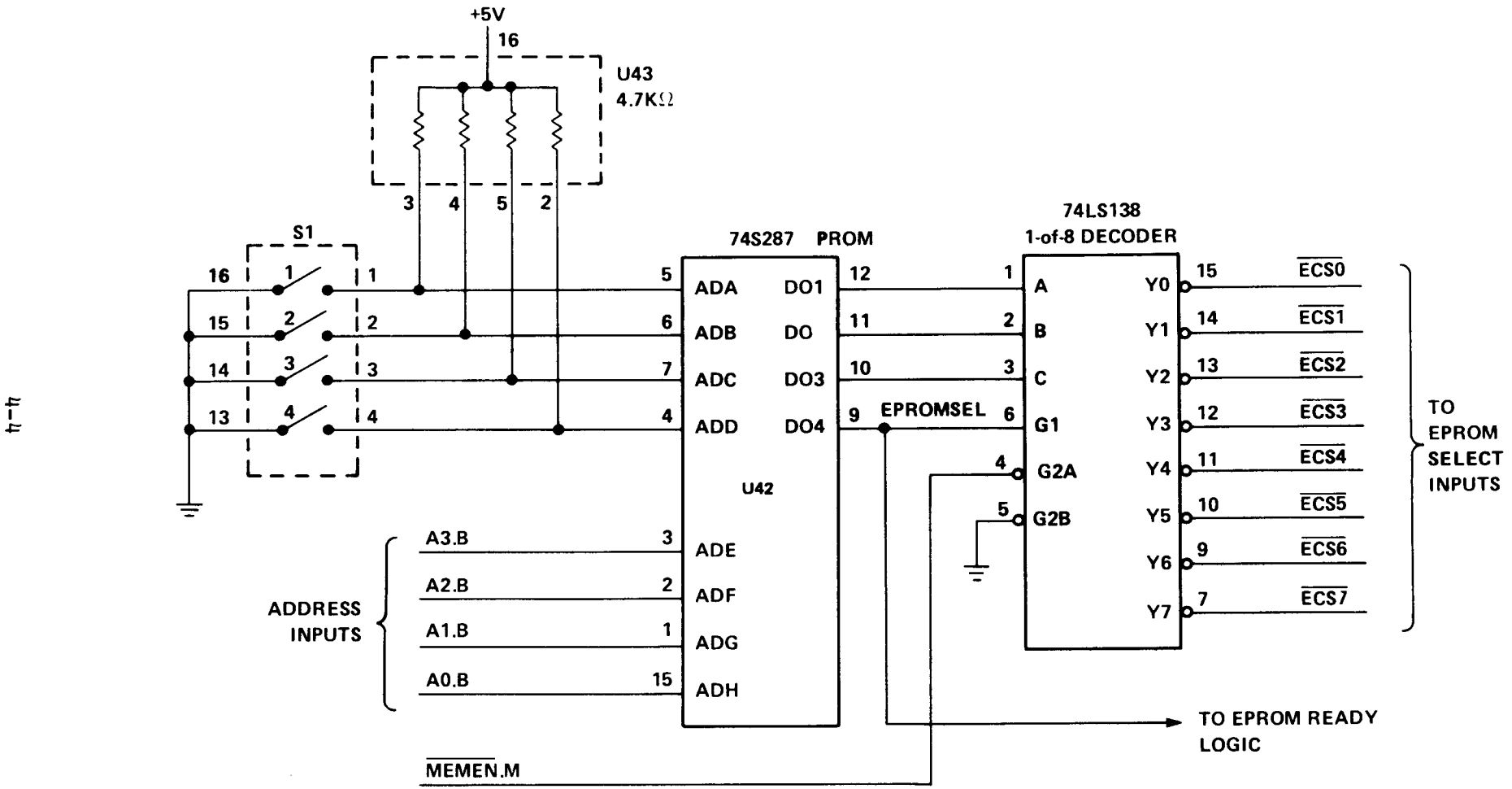


FIGURE 4-3. EPROM DECODE LOGIC

4.6 RAM DECODE LOGIC

Figure 4-4 is the logic diagram of the RAM decode logic. S1 switch positions 5 through 8 select a 16 by 4 block of memory in the 74S287 PROM. Each of the 16 blocks in the PROM corresponds to one of the 16 RAM address maps. Each nibble in the block diagram determines:

1) If a block of RAM is to be selected during the current memory cycle given the state of address lines A0 to A3.

2) Which block of RAM (RBLK0 to RBLK3) is selected.

The two least significant bits of the nibble (D01 and D02) coupled with address bit 4(EA4) from the microcomputer drive the 1-of-8 decoder in selecting one of the eight 1K x 16-bit banks of RAM. The most significant data bit of the nibble, D04, enables the decoder along with the memory enable signal (MEMEN.M) from the microcomputer. The outputs of the decoder are the select lines to the RAM banks.

The G2B input to the 74LS138 gates the RAM select lines so that no bus conflicts occur between the EPROM and RAM data buffers on the TM 990/201. This is accomplished with NORing the write strobe (WE.M) and data bus in (DBIN) from the microcomputer (detail is shown in Figure 4-8).

4.7 ADDRESSING SUMMARY

- The user has an option of 16 configurations each for RAM and EPROM, and a code OFF-OFF-OFF-OFF at S1 allows the user to disable the memories. These options are explained in detail in Section 3.

- The user has the option of programming his own decode configuration, placing memory on any 2K-word boundary. See Appendix A for details.

- An overlap of RAM and EPROM on board results in RAM dominance. See caution on page 3-2 for overlap from board to board.

4.8 MEMORY SPEED AND TIMING

This section describes memory speed and outlines timing for the TM 990/201 memory board.

4.8.1 Memory Speed

The TMS 9900 interfaces easily with slow memories. This is accomplished through the use of the "wait state" concept. During each memory cycle, the microprocessor samples the READY signal. When READY is active high, it indicates to the microprocessor that memory will be ready to read or write during the next clock cycle. When not-ready is indicated during a memory operation, the TMS 9900 enters a wait state and suspends internal operation until the memory system indicates it is ready to proceed.

The READY signal is generated on the TM 990/201 expansion memory board separately for RAM and EPROM. The board will be populated with TMS 2716 EPROM's that have an access time of 450 ns and 2114 static RAM's that have an access time in accordance with Table 1-1. At 3 MHz, the EPROM's and RAM's with access times in excess of 300 ns require one wait state. There are jumper provisions on the board to disable READY for RAM, EPROM, or both.

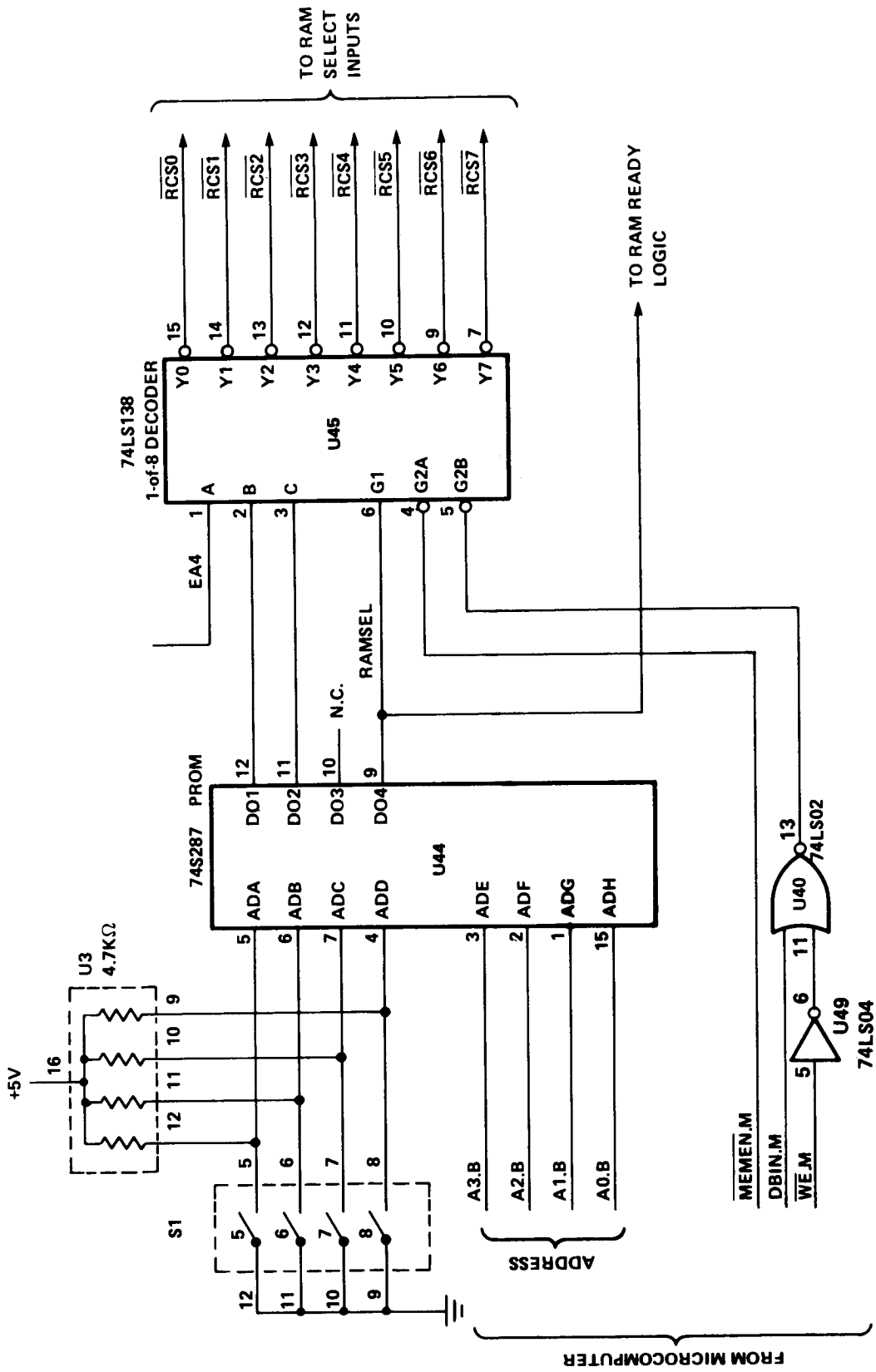


FIGURE 4-4. RAM DECODE LOGIC

Jumper J1 designates the memory speed for RAM used, and jumper J2 designates the EPROM speed. Table 4-1 shows the necessary jumper setting according to clock used and memory access time.

TABLE 4-1. FAST/SLOW JUMPER (J1/J2) POSITIONS VERSUS MEMORY ACCESS TIME

Access Time	CPU Operation	
	3 MHz	5 MHz
450 ns	SLOW	SLOW
300 ns	FAST	SLOW
200 ns	FAST	FAST
150 ns	FAST	FAST

Figures 1-1 and 4-5 show the jumper positions on the board for RAM (J1) and EPROM (J2). The jumpers are in the SLOW position; this is how the board is shipped. The TM 990/201-44 is shipped with J1 in the "FAST" position.

The speed setting for RAM and EPROM are for all RAM or all EPROM; therefore, if the addition or replacement of memories becomes necessary, the user must take into account the speed of the devices used. If the access time of the slowest RAM being added is more than 300 ns, the RAM jumper must be placed in the SLOW position. This assumes 3 MHz operation. Refer to Table 4-1 for the proper settings. If the RAM suplied with the board operates in the "FAST" mode and the jumper in the "SLOW" position, system performance will be less than optimal.

4.8.2 Memory Timing

The memory timing for the TM 990/201 board is shown in Figure 4-6. Memory write timing is shown with one wait state and read cycle timing is shown with none.

Care must be taken when interfacing the 2114 static RAM to the TMS 9900. During a write cycle, the chip select (S-) to the RAM's must be held high (inactive) until after WE- goes low. Otherwise the RAM's enter a read mode and enable their output buffers. The output buffers in the RAM's would fight against the data bus drivers and data would be lost. This condition would persist for approximately 1 clock cycle until WE- is output by the TMS 9900 microprocessor.

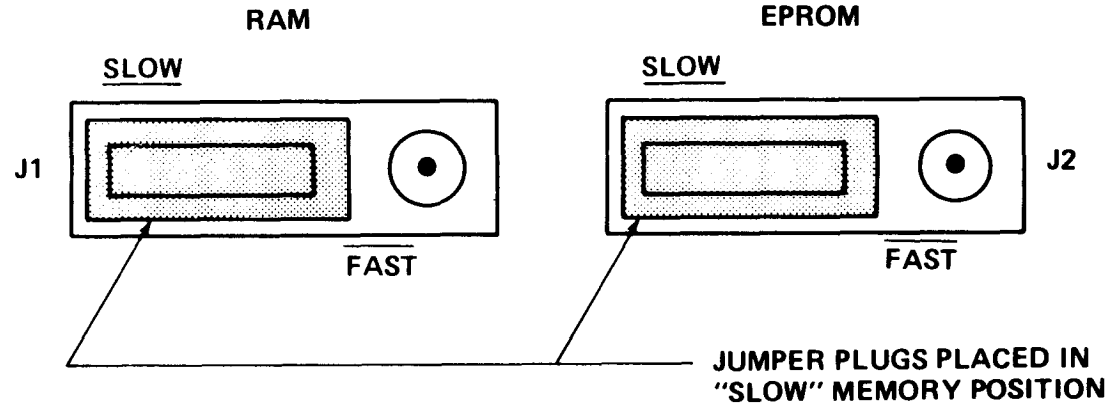


FIGURE 4-5. SLOW/FAST MEMORY JUMPER PLACEMENT

Note: Only RAM jumper J1 provided on the TM 990/206 board.

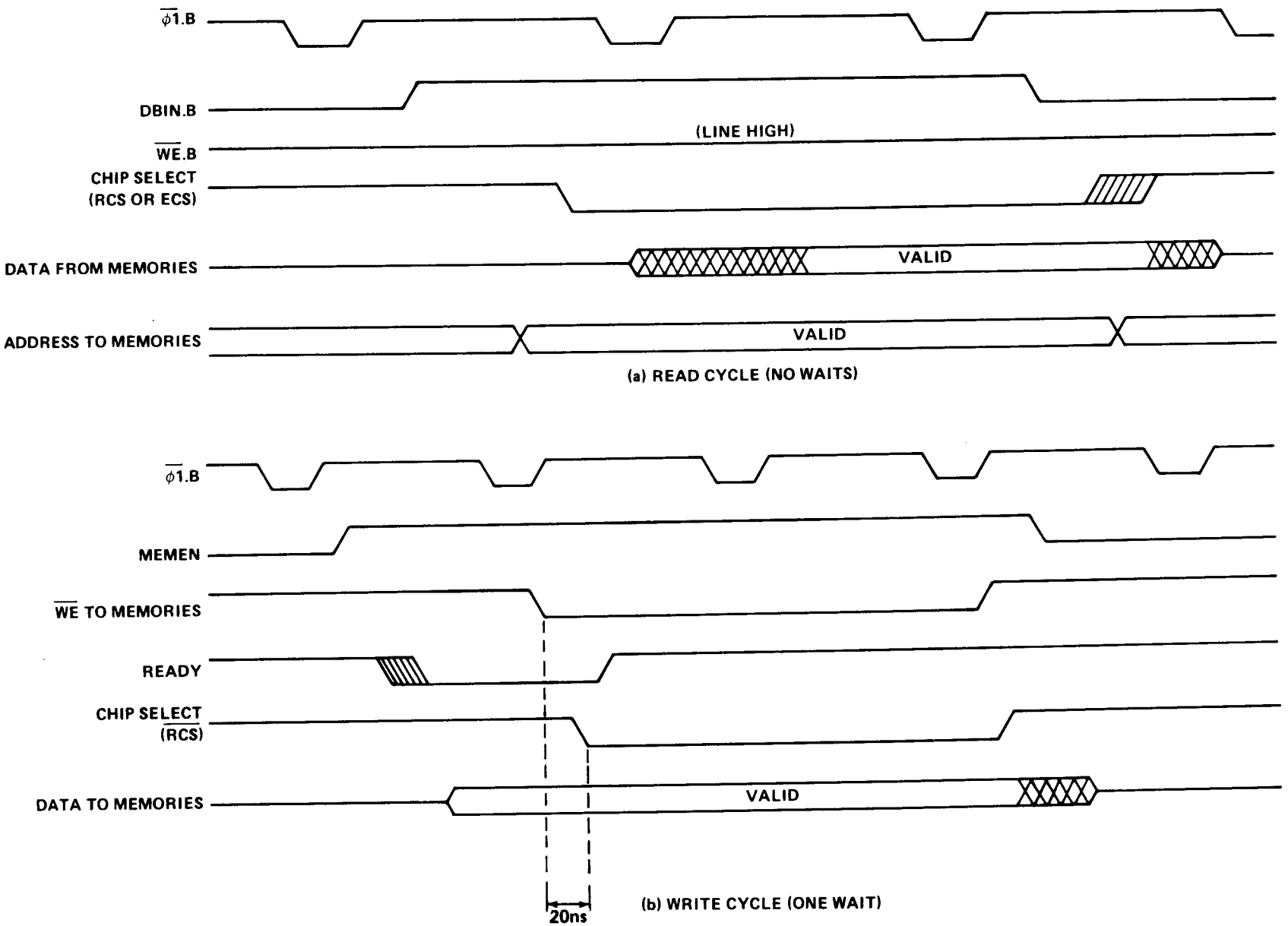


FIGURE 4-6. TM 990/201 MEMORY TIMING

The hardware on the TM 990/201 memory board resolves this problem. In essence the S- signal to the RAM's is an "OR"ed function of WE and DBIN. This method is recommended whenever devices with common I/O pins are used.

4.8.3 READY Logic

Figure 4-7 depicts the circuitry for the RAM READY logic. The EPROM READY logic is identical. The READY logic forces one wait state during each memory cycle the RAM is accessed.

If jumper J1 is in the FAST position, READY is never asserted low since the left flip-flop's CLR input is always low. Thus READY is never forced low. If J1 is in the SLOW position, READY is forced low for the first ø 1 clock period of every RAM memory cycle. The two flip-flops force READY high for the second and third clock cycles as shown in the timing diagram in Figure 4-6.

4.9 RAM PRECEDENCE LOGIC

Figure 4-8 details the RAM precedence logic. During any memory cycle that both RAM and EPROM are selected on the TM 990/201, the EPROM data buffers are placed in the high impedance state. Thus the RAM data buffers are the only buffers allowed to use the data bus.

4.10 INTERFACE DESCRIPTION

All of the interface functions for the TM 990/201 memory board are through the chassis backplane. A pin assignment chart is shown in Table 4-2. The signals used are shown with their corresponding pin number on the P1 connector tab.

Figure 4-9 shows the TM 990/510A chassis backplane.

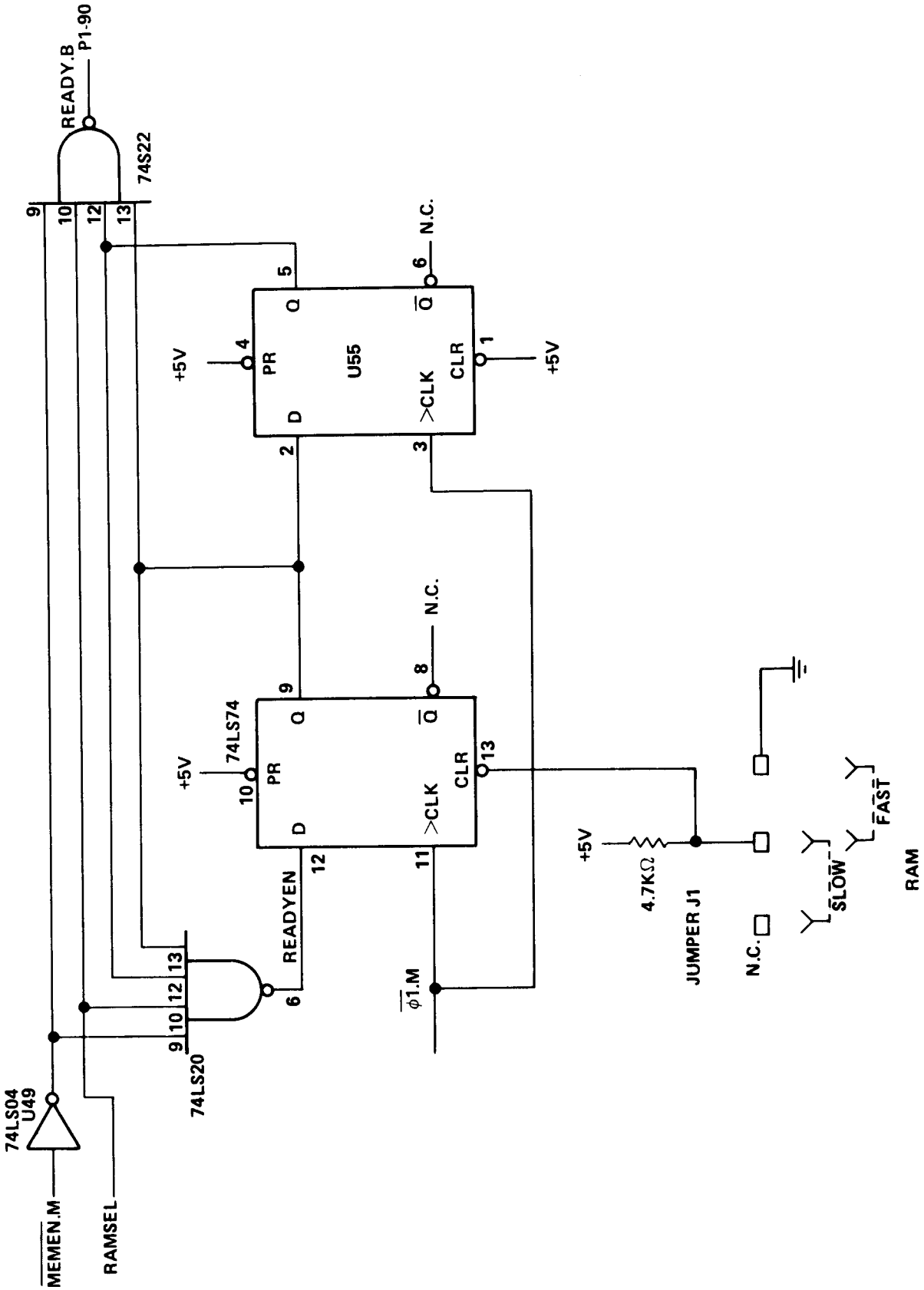


FIGURE 4-7. TM 990/201 RAM READY LOGIC

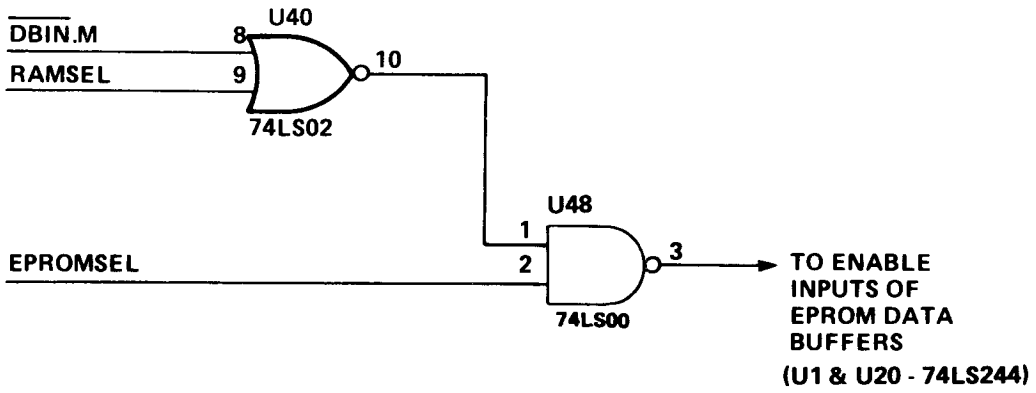


FIGURE 4-8. RAM PRECEDENCE LOGIC

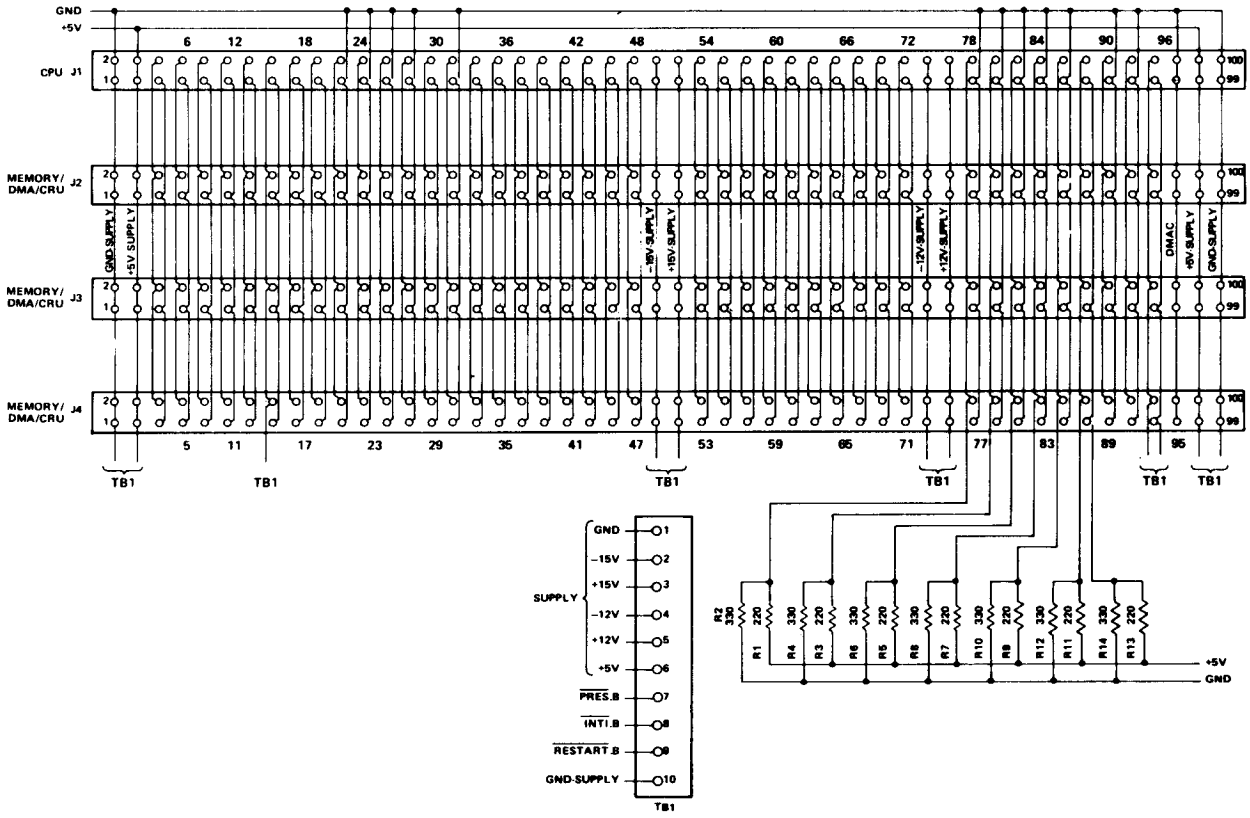


FIGURE 4-9. TM 990/510A OEM CHASSIS BACKPLANE SCHEMATIC