TEXAS INSTRUMENTS

TM 990

TM 990/101M Microcomputer User's Guide

SCANS OF SELECTED PAGES

MICROPROCESSOR SERIES™

May 1980

SECTION 1

INTRODUCTION

1.1 GENERAL

The Texas Instruments TM 990/101M is a self-contained microcomputer on a single printed-circuit board. The board's component side is shown in Figure 1-1, which also highlights major features and components. Figure 1-2 shows board dimensions. This microcomputer board contains features found on computer systems of much larger size, including a central processing unit (CPU) with hardware multiply and divide, programmable serial and parallel I/O lines, external interrupts, and a debug-monitor to assist the programmer in program development and execution. Other features include:

- TMS 9900 microprocessor based system: the microprocessor with the minicomputer instruction set - software compatible with other members of the 990 family.
- 1K x 16 bits of TMS 4045 random-access memory (RAM) expandable on-board to 2K x 16 bits.
- 1K x 16 bits of TMS 2708 erasable programmable read-only memory (EPROM), expandable on-board to 2K x 16 bits. Simple jumper modifications enable substitution of the larger TMS 2716 EPROM's (16K bits each) for the smaller TMS 2708's (8K bits each). Four TMS 2716's permit EPROM expansion to 4K x 16 bits.

  NOTE

  Three board configurations are available. The characteristics of each configuration are explained in paragraph 1.3.

- Buffered address, data, and control lines for off-board memory and I/O expansion; full DMA capabilities are provided by the buffer controllers.
- 3 MHz crystal-controlled clock.
- One 16-bit parallel I/O port, each bit is individually programmable.
- Modified EIA RS-232-C serial I/O interface, capable of communication to both EIA-compatible terminals and popular modems (data sets).
- A local serial I/O port, with interfaces for an EIA terminal and either a Teletype (TTY) or a twisted-pair balanced-line multidrop system (interface choices are detailed in paragraph 1.3).
- Three programmable interval timers.
- 17 prioritized interrupts, including RESET and LOAD functions. Interrupt 6 is level triggered (active LOW) and edge-triggered (either polarity) and latched on-board.
- A directly addressable five-position DIP switch and an addressable light emitting diode (LED) for custom system applications.
- PROM memory decoder permits easy reassignment of memory map configuration; see Figure 1-3 for memory map of the standard board.

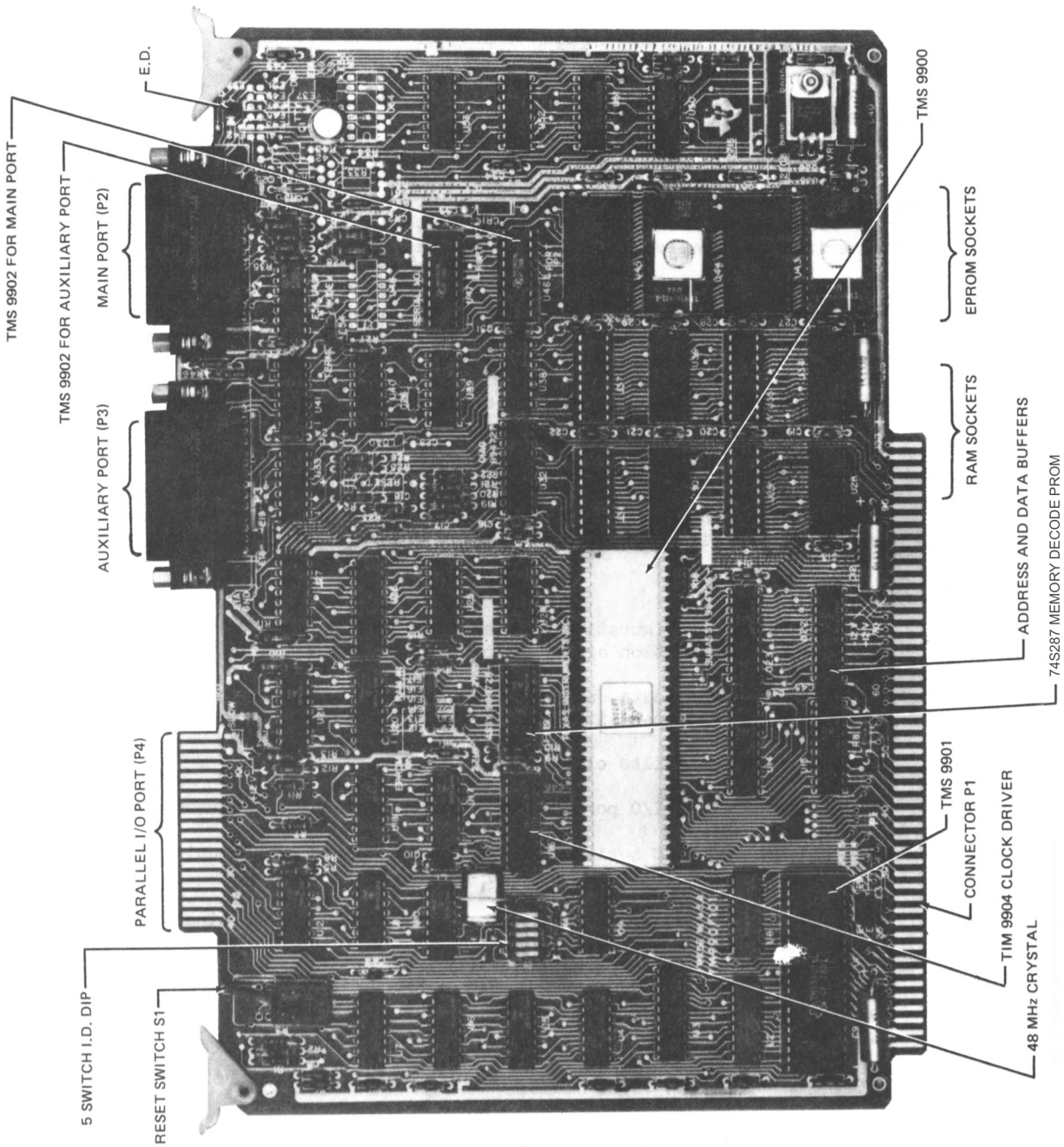


FIGURE 1-1 – TM990/101M MAJOR COMPONENTS

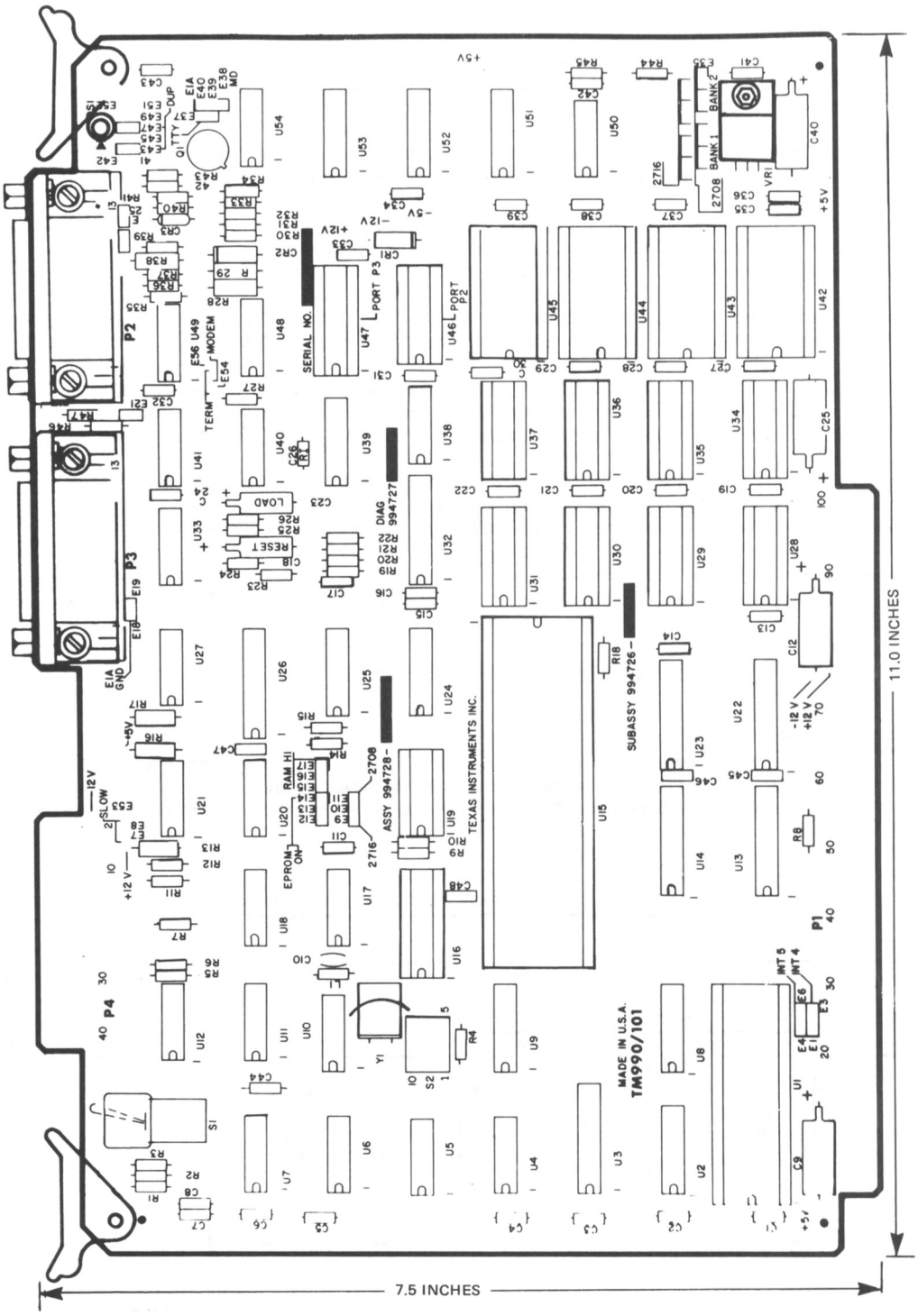


Figure 1-2. TM 990/101M Dimensions and Component Placement

1.2 MANUAL ORGANIZATION

Section 1 covers board specifications and characteristics. A glossary in paragraph 1.7 explains terms used throughout the manual.

Section 2 explains how to install, power-up, and operate the TM 990/101 microcomputer with the addition of a data terminal, power supplies, and appropriate connectors.

Section 3 explains how to communicate with the TM 990/101M using the TIBUG monitor. This versatile monitor, complete with supervisor calls and operator communication commands, facilitates the development and execution of software.

Section 4 describes the instruction set of the TM 990/101M, giving examples of each class of instructions and providing some explanation of the TMS 9900 architecture.

Section 5 explains basic programming procedures for the microcomputer, giving an explanation of the programming environment and hardware-dependent features. Numerous program examples are included for utilizing the various facilities of the TM 990/101M.

Section 6 is a basic theory of operation, explaining the hardware design configuration and circuitry. This section provides explanations of the bus structure, the control logic, and the various subsystems which make up the microcomputer.

Section 7 describes various options available for the microcomputer, both those supplied on-board and those which Texas Instruments offers for off-board expansion of the system.

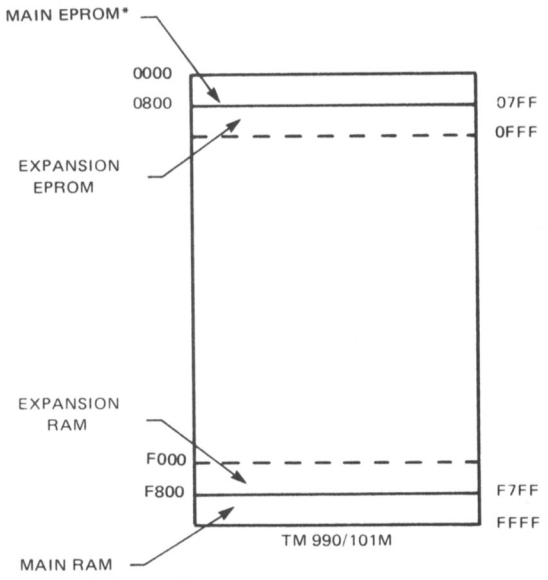
Section 8 features various hardware applications which can be built using the TM 990/101M.

1.3 PRODUCT INDEX

The TM 990/101M microcomputer is available in three different configurations, which are specified by a "dash number" appended to the product name; e.g., TM 990/101M-1. These configurations are listed in Table 1-1. A memory map is shown in Figure 1-3.

Table 1-1. TM 990/101M Configurations

TM 990/101M Dash No.	EPROM		RAM	Main Serial Port Option (EIA Terminal I/F Stand)
	Socketed	Program		
-1	2 TMS 2708 (1K x 16)	TIBUG Monitor	4 TMS 4045 (1K x 16)	TTY
-2	2 TMS 2716 (2K x 16)	Blank	4 TMS 4045 (1K x 16)	Multidrop
-3	4 TMS 2716 (4K x 16)	Blank	8 TMS 4045 (2K x 16)	TTY



*EPROM's programmed with TIBUG monitor.

Figure 1-3. Main And Expansion EPROM and RAM

1.4 BOARD CHARACTERISTICS

Figure 1-1 shows the major portions and components of the microcomputer. The system bus connector is P1, which is a 100-pin (50 each side) PC board edge connector spaced on 0.125 inch centers. Connector P2 is the main serial port and P3 is the RS-232-C auxiliary serial port. Both connectors are standard 25-position female jacks used in RS-232-C communications. The parallel I/O port is PC board edge connector P4, which has 40 pins (20 each side) spaced on 0.1-inch centers.

Figure 1-2 shows the PC board silkscreen markings which detail the various components on the board; also included are the board dimensions and tolerances.

1.5 GENERAL SPECIFICATIONS

	+5 V		+12 V		-12 V	
Power Consumption	TYP	MAX	TYP	MAX	TYP	MAX
TM 990/101M-1	1.8	2.6	0.30	0.50	0.25	0.40
TM 990/101M-2	1.8	2.6	0.30	0.50	0.25	0.40

Clock Rate: 3 MHz

Baud Rates (set by TIBUG): 110, 300, 600, 1200, 2400, 4800, 9600, 19200

Table 2-1. Board Jumper Positions As Shipped

Function	Stake Pins Used	Proper Connection & Description
Interrupt 4 source	E1,E2,E3	E1 to E2 - pin 18, connector P1
Interrupt 5 source	E4,E5,E6	E4 to E5 - pin 17, connector P1
Slow EPROM	E7,E8,E53	E8 to E53 - No WAIT state
2708/2716 Memory Map	E9,E10,E11	E10 to E11 - Use TMS 2708's
EPROM Enable	E12,E13,E14	E13 to E14 - On-board EPROM
HI/LO Memory Map	E15,E16,E17	E16 to E17 - EPROM low, RAM high
EIA Connector Ground	E18,E19	E18 to E19* - pin 1 of P3 grounded*
Microterminal +5 V	E20,E21	Shipped installed on -0001,3 only*
Microterminal +12 V	E22,E23	Shipped installed on -0001,3 only*
Microterminal -12 V	E24,E25	Shipped installed on -0001,3 only*
Main EPROM TYPE	E26 through E30	E27 to E28, E29 to E30 - TMS 2708's
Expansion EPROM type	E31 through E35	E32 to E33, E34 to E35 - TMS 2708's
Teletype	E36,E37	Shipped removed. On -0001,3 only, if using a TTY, borrow a Microterminal jumper plug for use here.
EIA/MD receive select	E38,E39,E40	E39 to E40 - EIA (and TTY) receive
Multidrop Termination	E41 through E52	Shipped installed on -0002 only*
Resistors and Duplex Select P3 Port Terminal/Modem	E54,E55,E56	E54 to E55 - Terminal Use*

*Jumper connection is not relevant for TIBUG operation with an RS-232-C or TTY terminal.

CAUTION

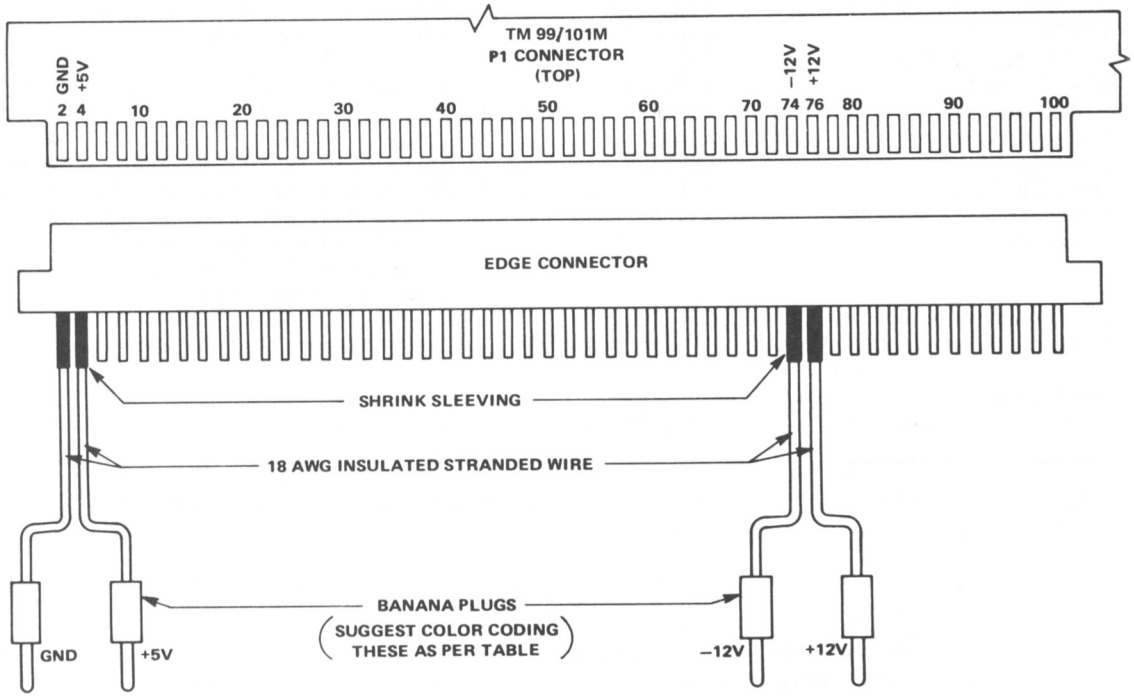
Be very careful to apply correct voltage levels to the TM 990/101M. Texas Instruments assumes no responsibility for damage caused by improper wiring or voltage application by the user.

2.4.1 POWER SUPPLY CONNECTIONS

Figure 2-1 shows how the power supply is connected to the TM 990/101M through connector P1, using a 100-pin edge connector. Be careful to use the correct pins as numbered on the board; these pin numbers may not correspond to the numbers on the particular edge connector used. Check connections with an ohmmeter before applying power if there is any doubt about the quality or location of a connection.

The table in Figure 2-1 shows suggested color coding for the power supply plugs. To prevent incorrect connection, label the top side of the edge connector "TOP" and the bottom "TURN OVER".

Figure 2-2 shows how to correctly place the TM 990/101M in the TM 990/510 card chassis. Slot 1 of the chassis is reserved for the microcomputer because termination resistors for the control bus signals are at the opposite end of the backplane, according to transmission line concepts. Slide the microcomputer into the slot, following the guides. Be sure the P1 connector is correctly aligned in the socket on the backplane, then gently but firmly push the board edge into the edge connector socket.



VOLTAGE	P1 PIN*	SUGGESTED PLUG COLORS
+5V	3, 4, 97, 98	RED
+12V	75, 76	BLUE
-12V	73, 74	GREEN
GND	1, 2, 99, 100	BLACK

*ON BOARD, ODD-NUMBERED PADS ARE DIRECTLY BENEATH EVEN-NUMBERED PADS.

A0001417

Figure 2-1. Power Supply Hookup

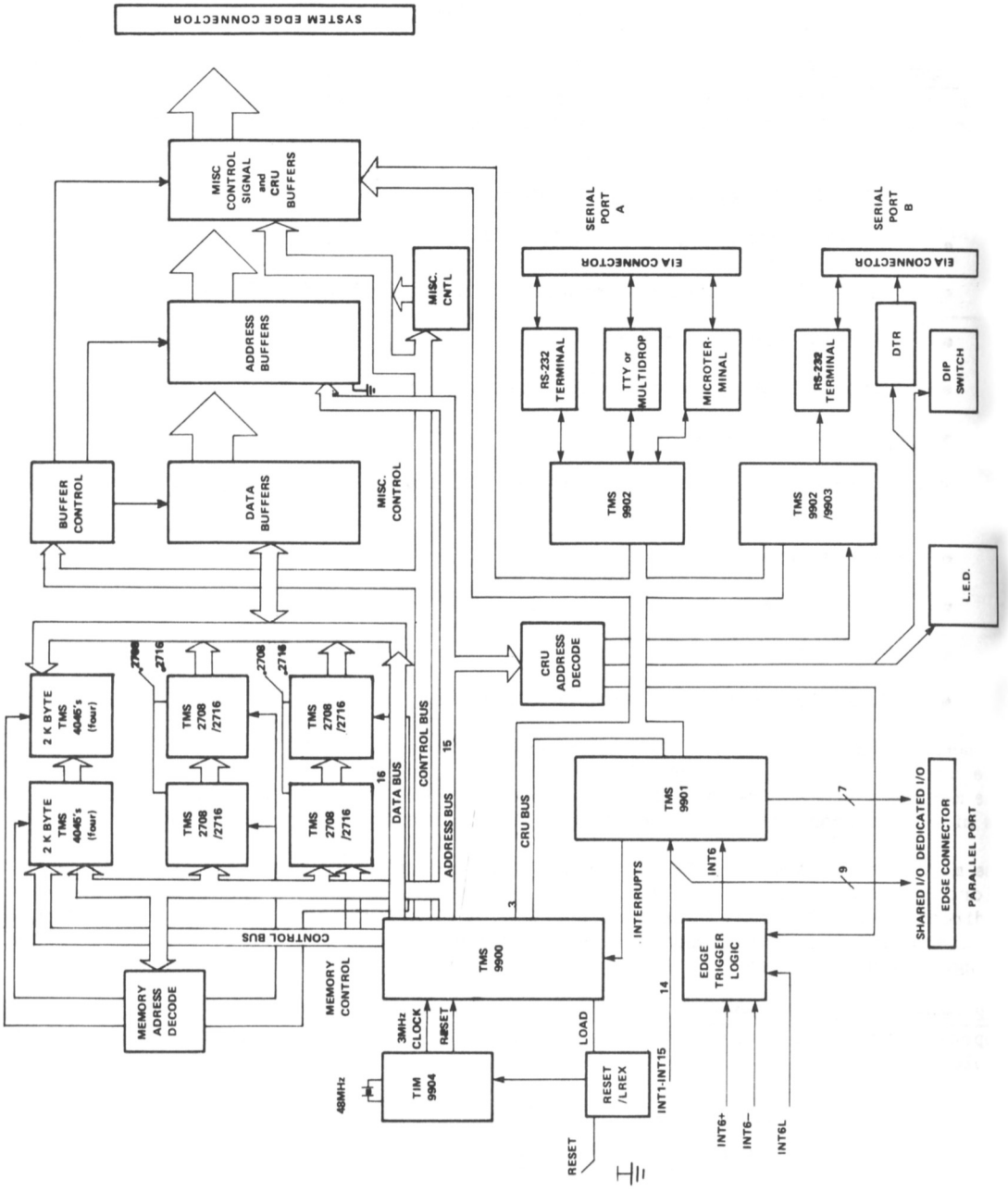


Figure 6-1. TM 990/101M Block Diagram

The supply -5V is derived on the board by the UA7905 regulator from the -12V line supplied from off board. The -5V supply is used primarily by the TMS 9900 microprocessor and the TMS 2708/2716 EPROM's for back-biasing the substrate, and by the multidrop interface as a supply voltage. The -12V supply is used for the EIA line drivers as well as for supplying the voltage to the -5V regulator.

The +12V supply is used by the TMS 9900 microprocessor and the TMS 2708/2716 EPROM's as the main voltage supply since these are MOS parts. The +12V also is used for the EIA line drivers.

All integrated circuits on the board, except the EIA line drivers, use the +5V supply, and because of the heavy load this voltage is not derived by an on-board regulator but must be supplied from off the board. The MOS parts use this supply for TTL compatibility, and, in fact, the TMS 9901, 9902, 9903, and 4045 use only this voltage for supply since they contain internal charge pumps, eliminating the need for -5 or +12V in their operation.

Table 6-1 lists the pin assignments of each integrated circuit for the supply voltages each uses.

Table 6-1. Device Supply Voltage Pin Assignments

Device	SUPPLY VOLTAGES TO PIN NUMBER				
	-12V	-5V	GND	+5V	+12V
TMS 9900		1	26,40	2,59	27
TMS 9901			16	40	
TMS 9902			9	18	
TMS 9902/03 socket			9	20	
TMS 9904			3,10	20	13
TMS 4045			9	18	
TMS 2708/2716		21	12	24	19
74LS241, 74LS245			10	20	
75188	1		7		14
75189			7	14	
75154			8	15	
75107		13	7	14	
75112		11	7	14	
74LS138, 153, 251, 259; 74S287			8	16	
74LSXX			7	14	

Figure 6-7. TM 990/101M Memory Addressing

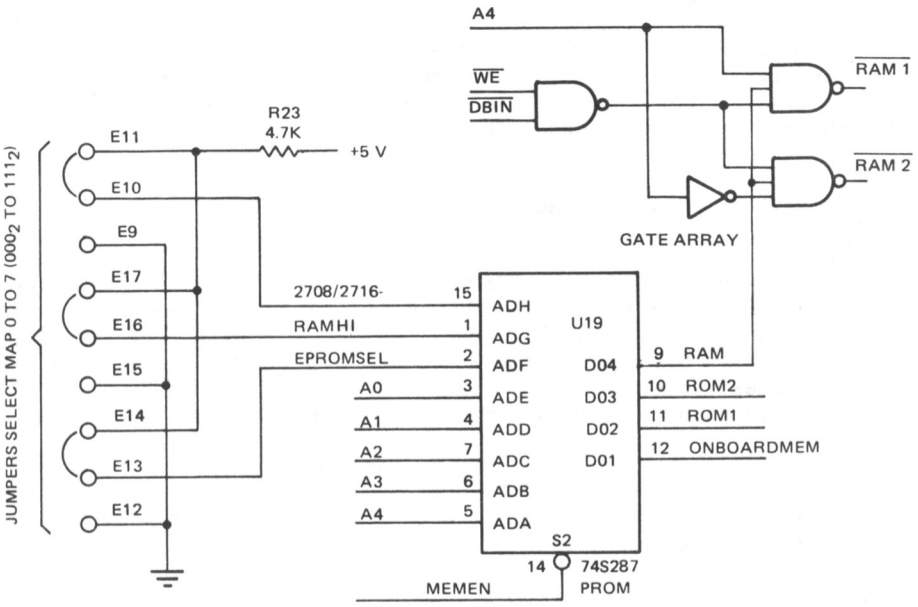


TABLE A. ADDRESS IN/DATA OUT

ADDRESS INPUT ADH TO ADA (LSB)	MAP	PROM OUTPUT (4 BITS EACH)							
00	0	66FF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
20	1	66FF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	CCAA
40	2	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FF66
60	3	CCAA	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FF66
80	4	66FF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
A0	5	66FF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFCA
C0	6	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FF66
E0	7	CAFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FF66

TABLE B. MAP CONFIGURATION (SET BY JUMPERS)

	2708 OR 2716 USED?	LOW OR HIGH RAM?	READ EPROM?
MAP 0 =	TMS 2716	Low RAM	No EPROM
Map 1 =	TMS 2716	Low RAM	High EPROM
Map 2 =	TMS 2716	High RAM	No EPROM
Map 3 =	TMS 2716	High RAM	Low EPROM
Map 4 =	TMS 2708	Low RAM	No EPROM
Map 5 =	TMS 2708	Low RAM	High EPROM
Map 6 =	TMS 2708	High RAM	No EPROM
Map 7 =	TMS 2708	High RAM	Low EPROM

Figure 6-8. Memory Address Decode PROM

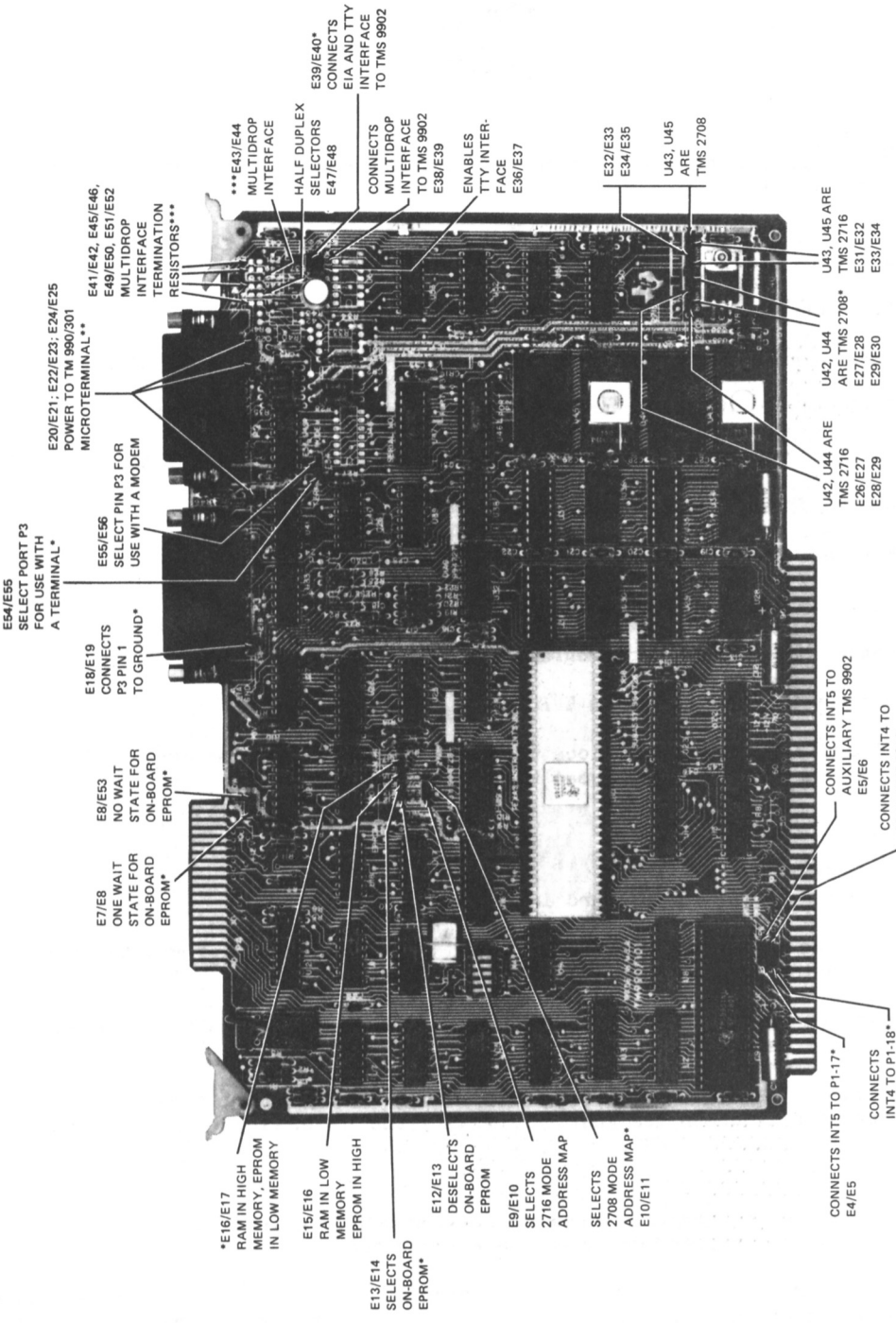


Figure 7-1. Jumper Placement

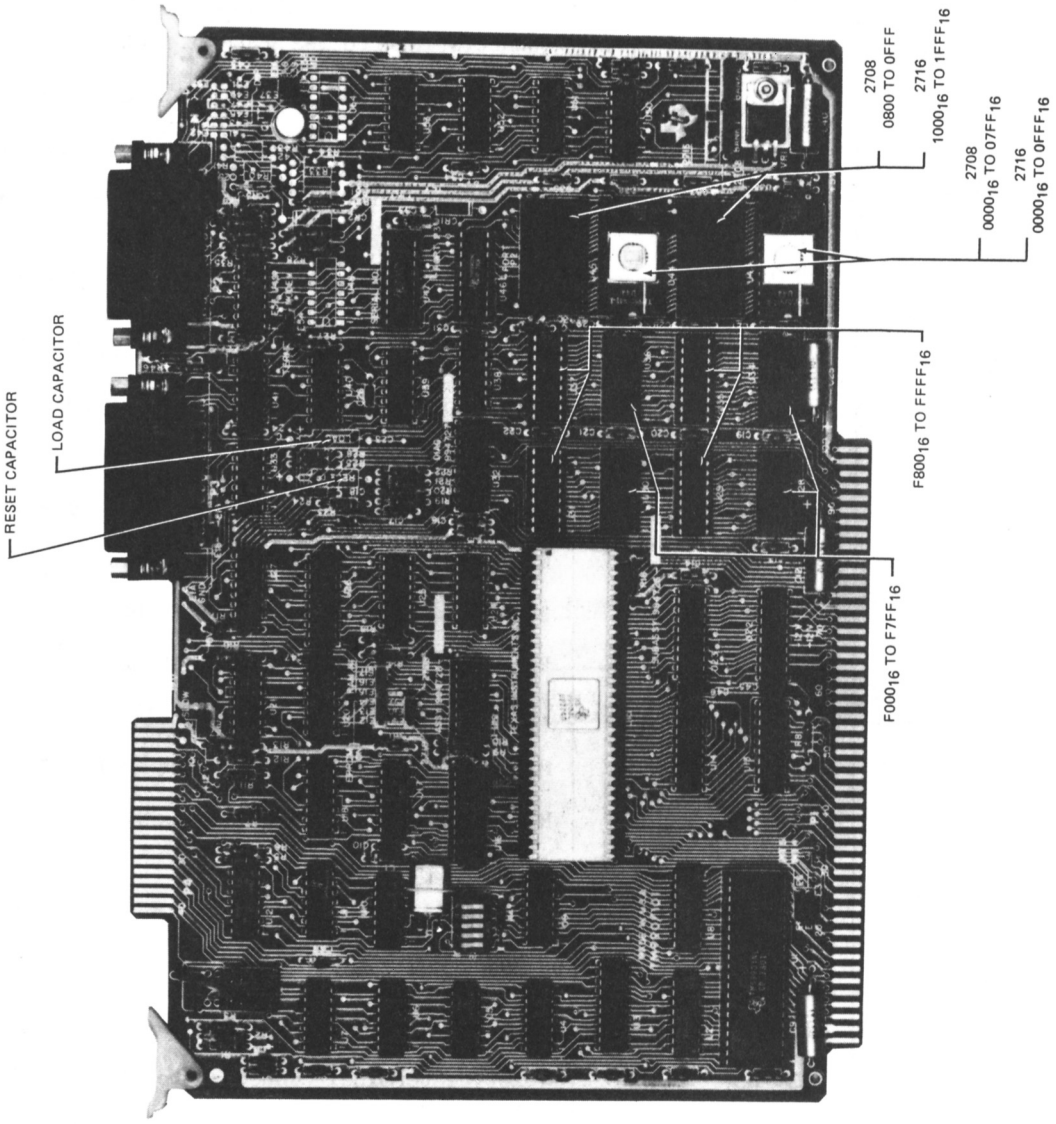


FIGURE 7-2 – MEMORY AND CAPACITOR PLACEMENT

Table 7-1. Master Jumper Table

No. Pins Staked	Pins Connected Together	Function When Connected
3	E1-E2	Connects INT 4 to pin 18 of P1 edge connector
	E2-E3	Connects INT4 to TMS 9902 of LOCAL I/O port
3	E4-E5	Connects INT5 to pin 17 of P1 edge connector
	E5-E6	Connects INT5 to TMS 9902 of REMOTE I/O port
3	E7-E8	Causes 1 WAIT state when on-board EPROM is accessed
	E8-E53	Causes no WAIT state: memory cycles are full speed
3	E9-E10	Selects memory map for TMS 2716 EPROM's
	E10-E11	Selects memory map for TMS 2708 EPROM's
3	E12-E13	On-board EPROM is disabled from memory map
	E13-E14	On-board EPROM is enabled into memory map
3	E15-E16	EPROM at high addresses, RAM in low
	E16-E17	EPROM at low addresses, RAM in high
2	E18-E19	Pin 1 of P3 is connected to GROUND
2	E20-E21	Microterminal: +5 volts to P2-14
2	E22-E23	Microterminal power: +12 volts to P2-12
2	E24-E25	Microterminal power: -12 volts to P2-13
5	E27-E28; E29-E30	Main EPROM is TMS 2708
	E26-E27; E28-E29	Main EPROM is TMS 2716
5	E32-E33; E34-E35	Expansion EPROM is TMS 2708
	E31-E32; E33-E34	Expansion EPROM is TMS 2716
2*	E36-E37	Teletype terminal connected to P2
3	E38-E39	Multidrop Interface in use with LOCAL I/O port
	E39-E40	EIA or TTY interface in use with LOCAL I/O port

Table 7-1. Master Jumper Table (Concluded)

No. Pins Staked	Pins Connected Together	Function When Connected
2 each**	E41-E42,E45-E46 E49-E50,E51-E52	Multidrop termination resistors connected
2 each**	E43-E44, E47-E48	Multidrop Half Duplex operation enabled
3	E54-E55	Connects TMS 9902 RTS to CTS for port P3 to communicate with an EIA compatible terminal.
	E55-E56	Connects TMS 9902 CTS to port P3 directly for communication with an EIA modem.

*On TM 990/101M-1 and -3 only
**On TM 990/101M-2 only

Table 7-2. Jumper Pins by Board Dash Number (Factory Installation)

Board Dash No.	Positions Staked	Jumper Installation at Factory (Positions)
-1, -3	E1-E40, E53-E56	E1-E2 E4-E5 E10-E11 E13-E14 E16-E17 E18-E19 E20-E21 E22-E23 E24-E25 E27-E28 E29-E30 E32-E33 E34-E35 E39-E40 E8-E53 E54-E55
-2	E1-E35, E38-E56	E1-E2 E4-E5 E10-E11 E13-E14 E16-E17 E18-E19 E27-E28 E29-E30 E32-E33 E34-E35 E39-E40 E41-E42 E43-E44 E45-E46 E47-E48 E49-E50 E51-E52 E8-E53 E54-E55

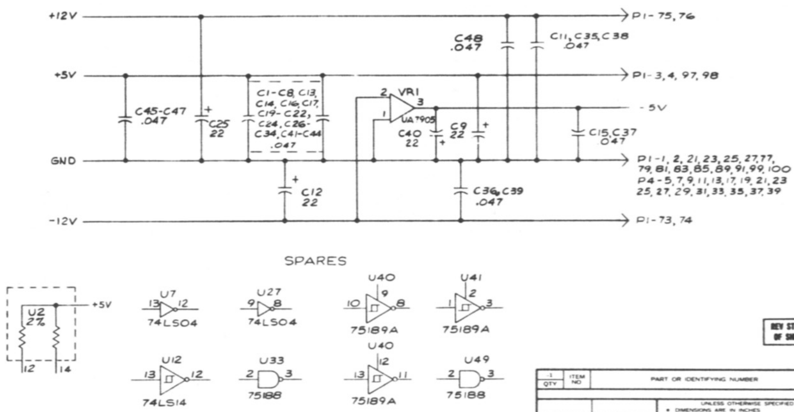
NOTES: UNLESS OTHERWISE SPECIFIED
1. CAPACITANCE VALUES ARE IN MICROFARADS
2. RESISTANCE VALUES ARE IN OHMS
3. ALL RESISTORS ARE 1/4 W, 5%
4. C18 AND C23 ARE USER'S OPTION
5. PIN NUMBER ASSIGNMENTS FOR U47 APPLY TO THE 20 PIN SOCKET TO ENABLE USER TO INTERCHANGE THE TMS 9902 (18 PINS) WITH A TMS9903 (20 PIN) (USER'S OPTION)
6. JUMPER PLUGS ARE INSTALLED ON E20-E21, E22-E23, E24-E25 AS SHOWN ON -0001 ONLY
7. THESE COMPONENTS ARE INSTALLED ON -0001 ONLY
8. THESE COMPONENTS ARE INSTALLED ON -0002 ONLY
9. NC DENOTES NO CONNECTION

Device	Supply Voltages to Pin Number				
	-12 V	-5 V	GND	+5 V	+12 V
TMS 9900		1	26	2	27
TMS 9901			16	40	
TMS 9902			9	18	
TMS 9902/03 SOCKET			9	20	
TMS 9904			3,10	20	13
TMS 4045			9	18	
TMS 2708/2716		21	12	24	19
74LS241, 74LS245			10	20	
75188	1		7		14
75189			7	14	
75154			8	15	
75107		13	7	14	
75112		11	7	14	
74LS138, 153, 251, 259; 74S287			8	16	
74LS00			7	14	
74LS02			7	14	
74LS04			7	14	
74LS08			7	14	
74LS10			7	14	
74LS14			7	14	
74LS74			7	14	
74LS132			7	14	

DWG NO 994727 SH 1

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	REVISED TO AGREE W/ASSY	5/12/8	
B	CN430048 JERRY CLARK	7/05/78	
C	CN436599		
D	471723	4/7/80	



REV STATUS OF SHEETS	REV	D	C	D	A	A	C	D
	SH	1	2	3	4	5	6	7

PARTS LIST

QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	PROCUREMENT SPECIFICATION	NOTES

NEXT ASSY	USED ON
994726	8117
994728	8117

APPLICATION

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES

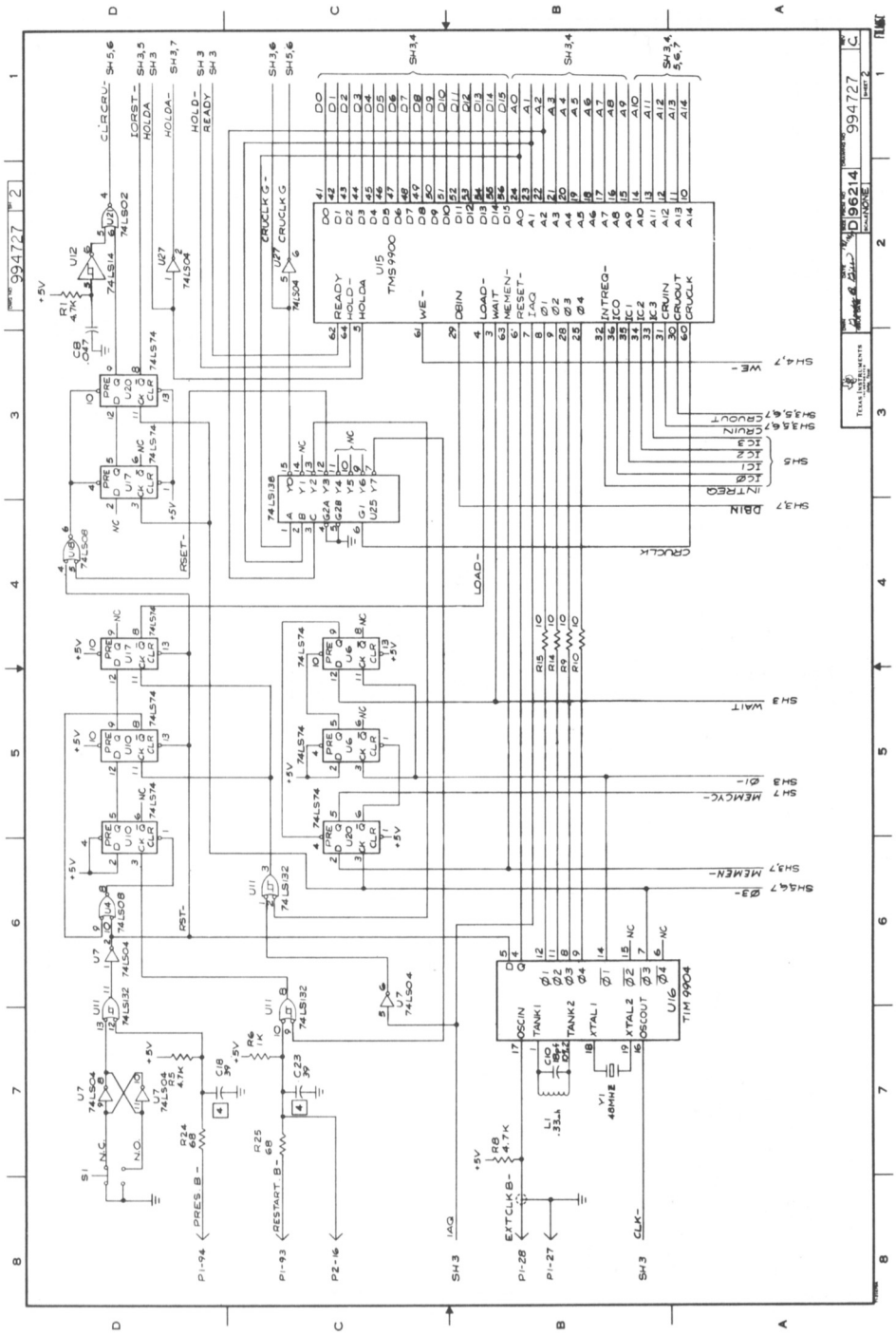
TEXAS INSTRUMENTS INCORPORATED Dallas, Texas

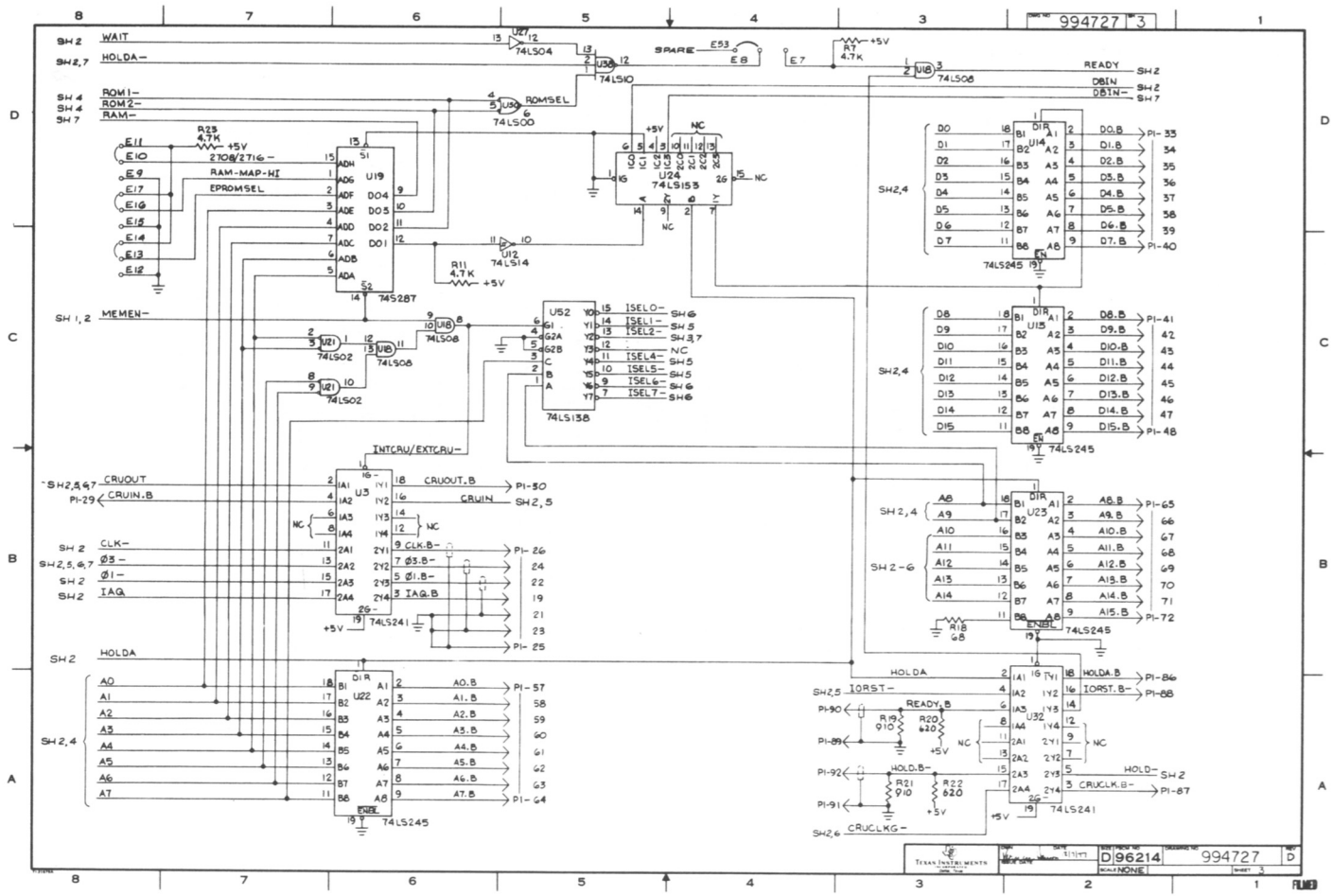
DIAGRAM, LOGIC, DETAILED TM990/101M

D 96214 994727 FILMED

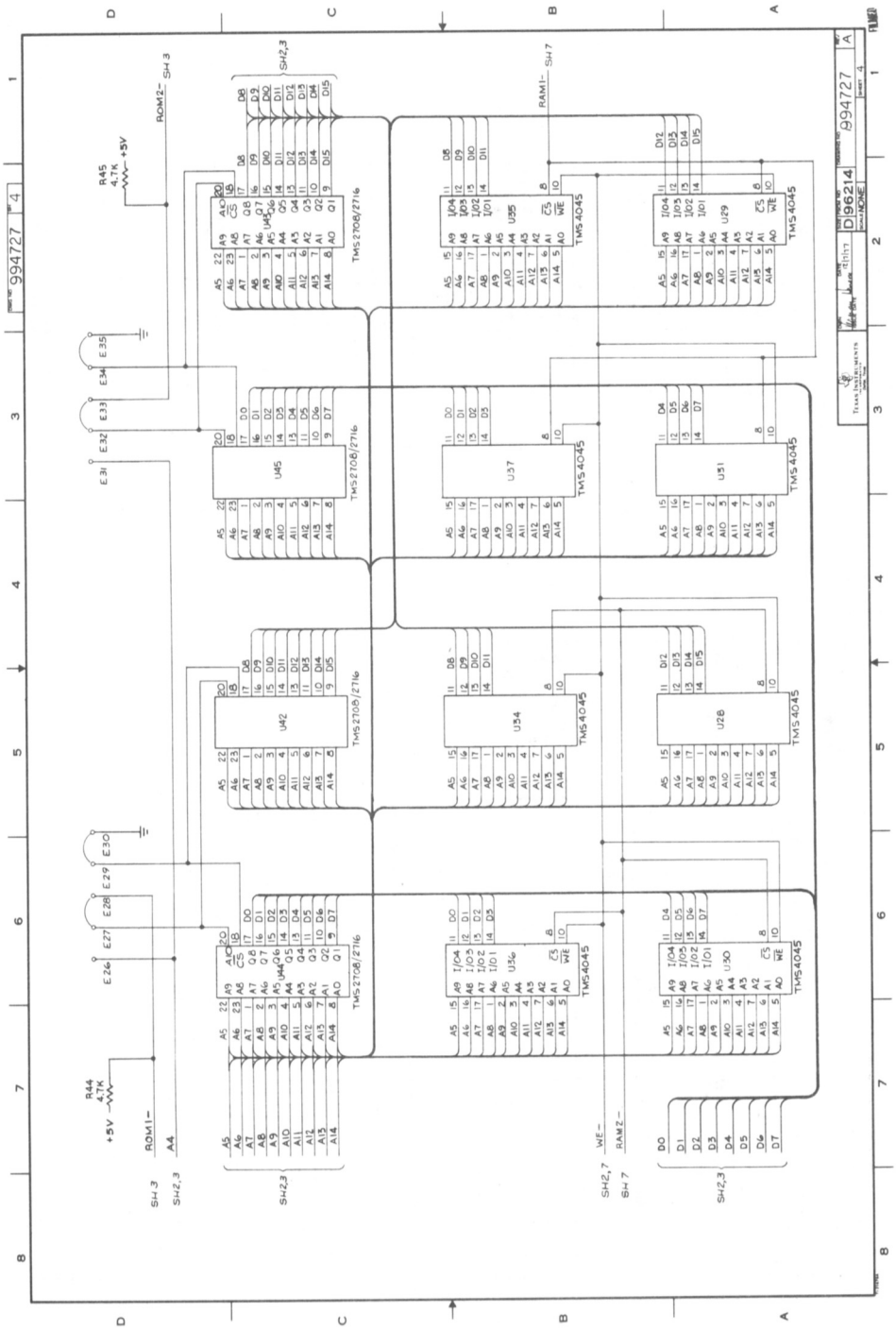
SCALE NONE SHEET 1 OF 7

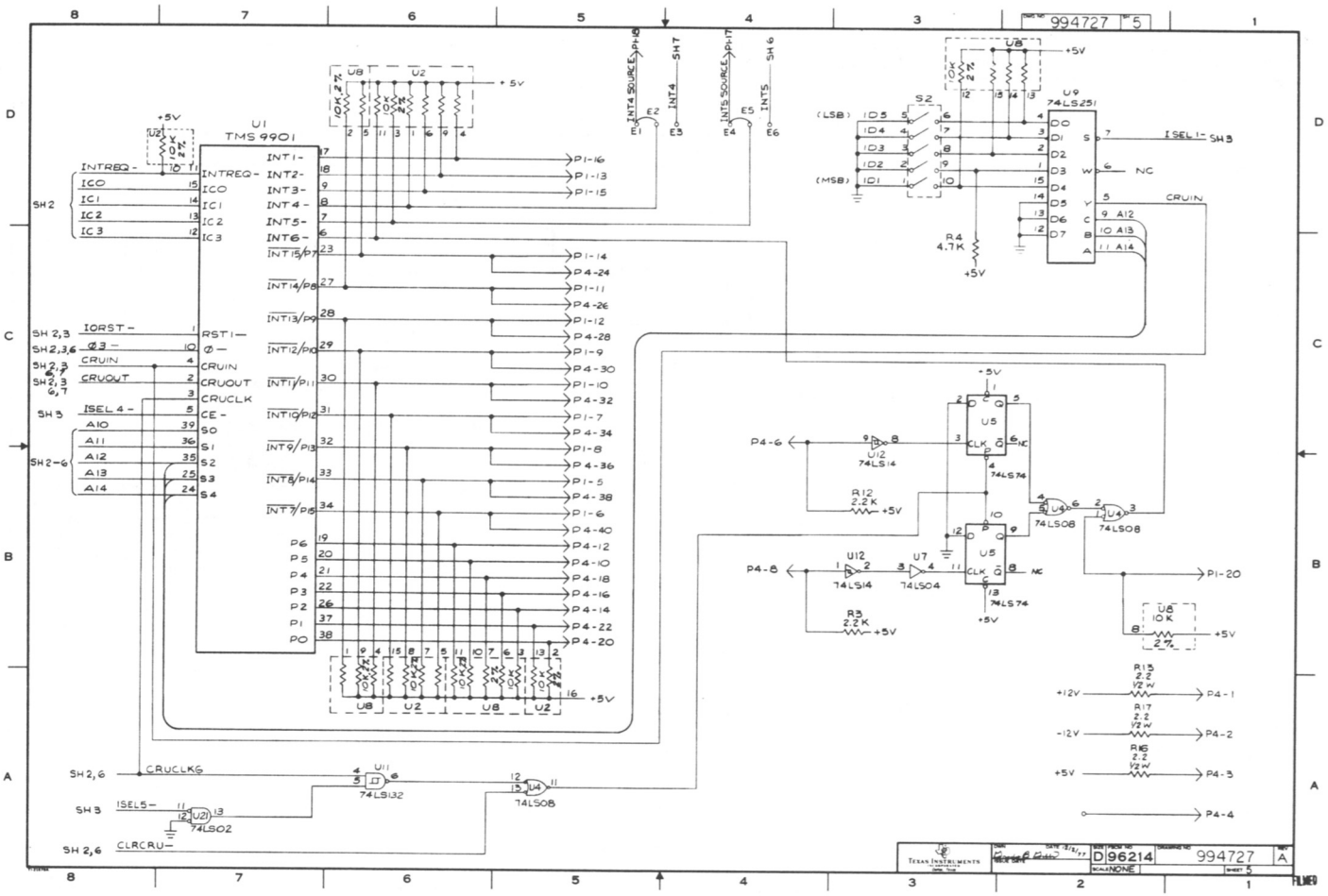
SEQ NO | IDENT | F.SPEC | NO | ADDITIONAL | NOTES
PROCESS | CLASSIFICATION
PROCESSES — FOR CORRELATION TO GOVT/IND SPECIFICATIONS SEE TI DRAWING 729467



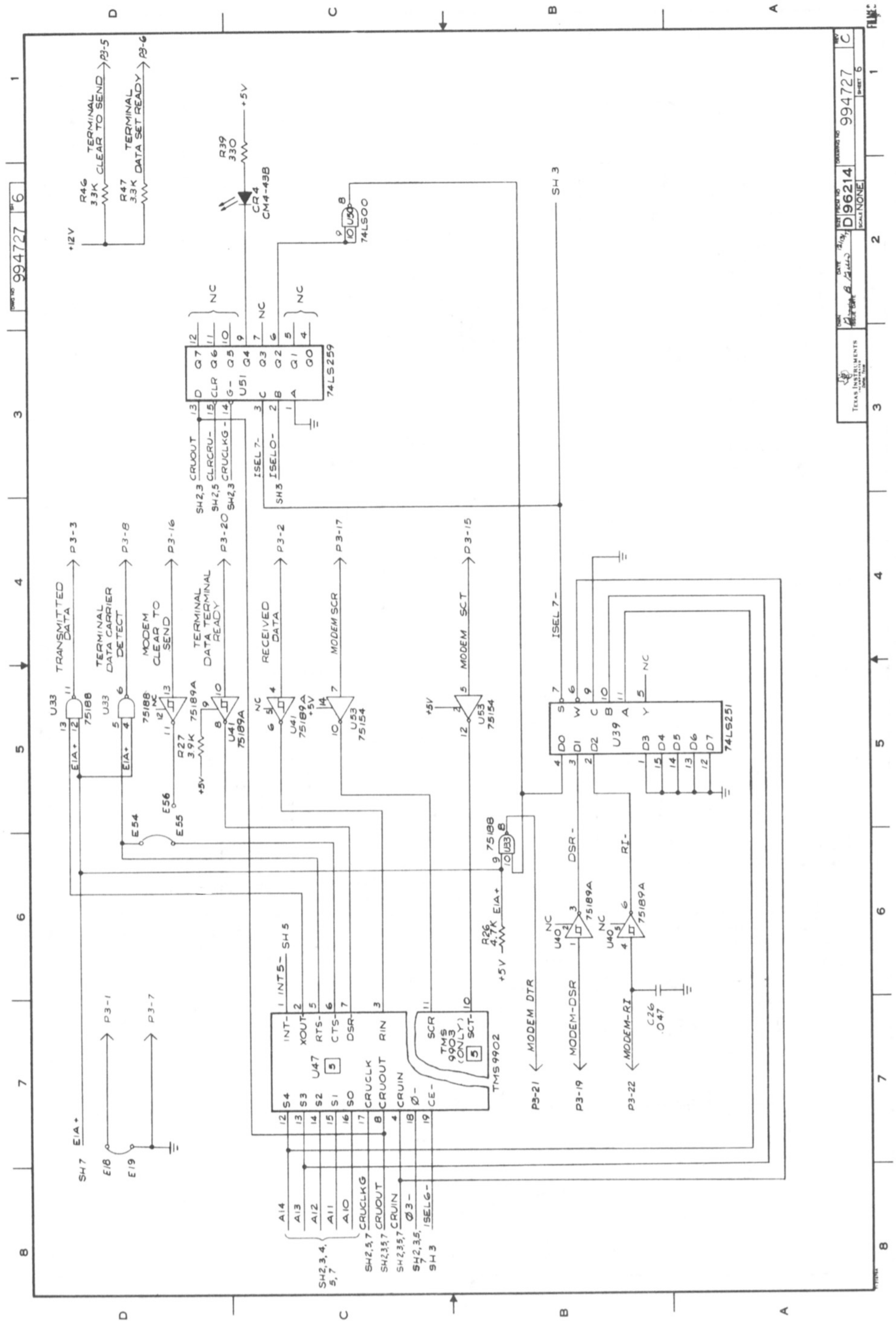

994727 3
WAIT
HOLDA–
ROM1–
ROM2–
RAM–
ROMSEL
74LS00
74LS04
74LS10
SPARE
E53
E8
E7
R7 4.7K
+5V
74LS08
READY
DBIN
R23 4.7K
2708/2716–
RAM-MAP-HI
EPROMSEL
74S287
R11 4.7K
74LS14
74LS153
NC
74LS245
MEMEN–
74LS02
74LS08
74LS138
ISEL0–
ISEL1–
ISEL2–
ISEL4–
ISEL5–
ISEL6–
ISEL7–
INTCRU/EXTCRU–
CRUOUT
CRUIN.B
CRUOUT.B
CRUIN
CLK–
Ø3 –
Ø1–
IAQ
74LS241
HOLDA
74LS245
IORST–
READY.B
HOLD.B–
CRUCLK.B–
CRUCLKG–
R18 68
R19 910
R20 620
R21 910
R22 620
D96214
994727
SCALE NONE

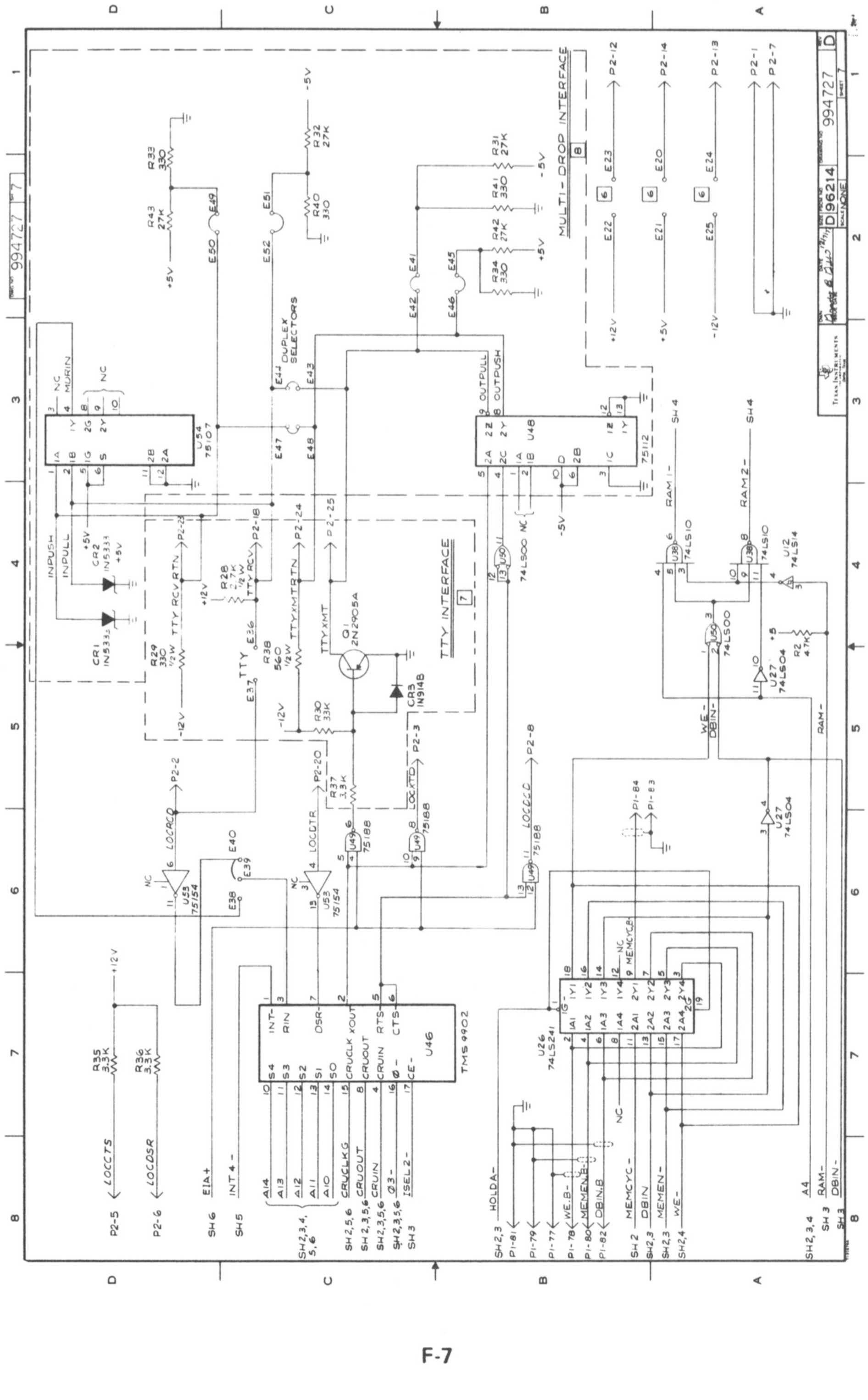
F-3




994727 5
U1
TMS 9901
INTREQ-
ICO
IC1
IC2
IC3
IORST-
Ø3-
CRUIN
CRUOUT
CRUCLK
ISEL 4-
A10
A11
A12
A13
A14
RST1-
Ø-
CE-
S0
S1
S2
S3
S4
INT1-
INT2-
INT3-
INT4-
INT5-
INT6-
P6
P5
P4
P3
P2
P1
P0
+5V
INT4 SOURCE
INT5 SOURCE
S2
(LSB) ID5
ID4
ID3
ID2
(MSB) ID1
U9
74LS251
ISEL1- SH3
NC
CRUIN
A12
A13
A14
R4
4.7K
U5
74LS74
U12
74LS14
U7
74LS04
74LS08
R12
2.2K
R3
2.2K
P1-20
R13
2.2
1/2 W
+12V
P4-1
R17
-12V
P4-2
R16
P4-3
P4-4
U11
74LS132
U21
74LS02
CRUCLKG
ISEL5-
CLRCRU-
D96214
994727
NONE
SHEET 5
A

F-5


994727
74LS259
74LS251
TMS9902
75188
75189A
75154
74LS00
TEXAS INSTRUMENTS


MULTI-DROP INTERFACE
TTY INTERFACE
DUPLEX SELECTORS
TMS 9902
U46
994727
D96214

APPENDIX H

P1, P2, AND P4 PIN ASSIGNMENTS

TABLE H-1. CHASSIS INTERFACE CONNECTOR (P1) SIGNAL ASSIGNMENTS

P1 PIN	SIGNAL	P1 PIN	SIGNAL	P1 PIN	SIGNAL
33	D0.B	71	A14.B	12	$\overline{\text{INT13}}$.B
34	D1.B	72	A15.B	11	$\overline{\text{INT14}}$.B
35	D2.B	22	$\overline{\text{Ø1}}$.B	14	$\overline{\text{INT15}}$.B
36	D3.B	24	$\overline{\text{Ø3}}$.B	28	EXTCLK.B
37	D4.B	92	$\overline{\text{HOLD}}$.B	3	+5V
38	D5.B	86	HOLDA.B	4	+5V
39	D6.B	82	DBIN.B	97	+5V
40	D7.B	26	$\overline{\text{CLK}}$.B	98	+5V
41	D8.B	80	$\overline{\text{MEMEN}}$.B	75	+12V
42	D9.B	84	$\overline{\text{MEMCYC}}$.B	76	+12V
43	D10.B	78	$\overline{\text{WE}}$.B	73	−12V
44	D11.B	90	READY.B	74	−12V
45	D12.B	87	$\overline{\text{CRUCLK}}$.B	1	GND
46	D13.B	30	CRUOUT.B	2	GND
47	D14.B	29	CRUIN.B	21	GND
48	D15.B	19	IAQ.B	23	GND
57	A0.B	94	$\overline{\text{PRES}}$.B	25	GND
58	A1.B	88	$\overline{\text{IORST}}$.B	27	GND
59	A2.B	16	$\overline{\text{INT1}}$.B	31	GND
60	A3.B	13	$\overline{\text{INT2}}$.B	77	GND
61	A4.B	15	$\overline{\text{INT3}}$.B	79	GND
62	A5.B	18	$\overline{\text{INT4}}$.B	81	GND
63	A6.B	17	$\overline{\text{INT5}}$.B	83	GND
64	A7.B	20	$\overline{\text{INT6}}$.B	85	GND
65	A8.B	6	$\overline{\text{INT7}}$.B	89	GND
66	A9.B	5	$\overline{\text{INT8}}$.B	91	GND
67	A10.B	8	$\overline{\text{INT9}}$.B	99	GND
68	A11.B	7	$\overline{\text{INT10}}$.B	100	GND
69	A12.B	10	$\overline{\text{INT11}}$.B	93	$\overline{\text{RESTART}}$.B
70	A13.B	9	$\overline{\text{INT12}}$.B		

TABLE H-2. SERIAL I/O INTERFACE (P2) PIN ASSIGNMENTS

P2 PIN	SIGNAL	DESCRIPTION
1	GND	
7	GND	
3	RS232 XMT	RS232 Serial Data Out
2	RS232 RCV	RS232 Serial Data In
5	CTS	Clear to Send (3.3KΩ pull-up to +12 V)
6	DSR	Data Set Ready (3.3KΩ pull-up to +12 V)
8	DCD	Carrier Detect
20	DTR	Data Terminal Ready
18,23	TTY XMT	TTY Receive Loop/Private Wire Receive Pair
24,25	TTY RCV	TTY Transmit Loop/Private Wire Transmit Pair
17	RCV CLK	Receive Clock
15	XMT CLK	Transmit Clock
12*	+12 V	Jumper Option for Microterminal
13*	−12 V	Jumper Option for Microterminal
14*	+5 V	Jumper Option for Microterminal
16	RESTART	Invokes the Load Interrupt to the TMS 9900 CPU

*When using the Microterminal, these voltages are jumpered to the corresponding pin in connector P2. Else, the voltages are not connected.

TABLE H.3 SERIAL I/O INTERFACE (P3) PIN ASSIGNMENTS

P3 PIN	SIGNAL	DESCRIPTION
1	OPTIONAL GND	GROUND IF JUMPER AT E18, E19
7	GND	GROUND
2	RS232 RCV	RS232 Serial Data In
3	RS232 XMT	RS232 Serial Data Out
5	CTS-Terminal	Terminal Clear to Send (3.3 kΩ pull-up to +12 V)
6	DSR-Terminal	Terminal Data Set Ready (3.3 kΩ pull-up to +12 V)
8	DCD-Terminal	Terminal Data Carrier Detect (activated by TMS 9902 Request to Send)
16	CTS-Modem	Modem Clear to Send*
19	DSR-Modem	Modem Data Set Ready*
20	DTR-Terminal	Terminal Data Terminal Ready
	DCD-Modem	Modem Data Carrier Detect*
21	DTR-Modem	Modem Data Terminal Ready*
15	$\overline{\text{SCT}}$	Synchronous Transmit Clock
17	SCR	Synchronous Receive Clock
22	RI	Ring Indicator

*Used with TM 990/506 Modem Cable Only.

TABLE H-4. PARALLEL I/O INTERFACE (P4) SIGNAL ASSIGNMENT

P4 PIN	SIGNAL	P4 PIN	SIGNAL
20	P0	17	GND
22	P1	15	GND
14	P2	13	GND
16	P3	11	GND
18	P4	9	GND
10	P5	39	GND
12	P6	37	GND
24	$\overline{\text{INT15}}$ or P7	35	GND
26	$\overline{\text{INT14}}$ or P8	33	GND
28	$\overline{\text{INT13}}$ or P9	31	GND
30	$\overline{\text{INT12}}$ or P10	29	GND
32	$\overline{\text{INT11}}$ or P11	27	GND
34	$\overline{\text{INT10}}$ or P12	25	GND
36	$\overline{\text{INT9}}$ or P13	23	GND
38	$\overline{\text{INT8}}$ or P14	21	GND
40	$\overline{\text{INT7}}$ or P15	19	GND
7	GND	1	+12 V
8	POSITIVE EDGE TRIGGER $\overline{\text{INT6}}$	2	−12 V
		3	+5 V
		4	SPARE
		5	GND
		6	NEGATIVE EDGE TRIGGER $\overline{\text{INT6}}$