Addendum to TM990/101MA Microcomputer User's Guide

2490275-0004

WARNING

To ensure that the equipment described by this manual, as well as all equipment connected to and used with it, operates satisfactorily and safely, all applicable local and national codes that apply to installing and operating the equipment must be followed. Since codes can vary geographically and can change with time, it is the user's responsibility to determine which standards and codes apply, and to comply with them.

FAILURE TO COMPLY WITH APPLICABLE CODES AND STANDARDS CAN RESULT IN DAMAGE TO EQUIPMENT AND/OR SERIOUS INJURY TO PERSONNEL.

All equipment should be installed and operated according to all applicable sections of the National Fire Code, National Electrical Code, and the codes of the National Electrical Manufacturer's Association (NEMA) as a minimum. Contact your local Fire Marshall and Electrical Inspector to determine which codes and standards apply to your specific case.

Personnel who are to install and operate the equipment should carefully study this manual and any others referred to by it prior to installation and/or operation of the equipment.

If you have any questions regarding the installation or operation of the equipment, or if more information is desired, contact your authorized Applications Engineering Distributor (AED) or the Texas Instruments Hot Line (615-461-2501).

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The specifications and descriptions contained in this manual were accurate at the time they were approved for printing. Since Texas Instruments Incorporated constantly strives to improve all its products, we reserve the right to make changes to equipment and/or manuals at any time without notice and without incurring any obligation other than as noted in this manual.

11/89

Addendum to TM990/101MA User's Guide

The TM990/101MA printed circuit board (PCB) has been upgraded to the TM990/101MB. This addendum highlights the changes made to the board. Continue to use the *TM990/101MA User's Guide,* along with the addendum. In the user's guide, change all TM990/101**MA** references to TM990/101**MB**.

NOTE

Throughout the addendum, references are made to figures and tables in the manual as well as in the addendum. References for figures and tables to be found in the manual are *italicized*.

1.1 GENERAL *(page 1-1)*

The Texas Instruments TM990/101MB is a self-contained microcomputer on a single PCB. The component side of the board is shown in *Figure 1-1* in the manual. The microcomputer contains features found in much larger computer systems including a Central Processing Unit (CPU) with hardware multiply and divide, programmable serial and parallel I/O lines, external interrupts, and a monitor to assist the programmer in program development and execution. Other features are included.

- TMS 9900 microprocessor-based system: software is compatible with other members of the TM990 family.
- 2K x 16 bits of HM6116 random-access memory (RAM) expandable to 8K x 16 bits.
- 8K x 16 bits of 2764 erasable programmable read-only memory (EPROM). Simple jumper modifications allow substitution of 2716, 2732, or 27128 devices.
- Three board configurations are available. The characteristics of each configuration are explained in *Section 1.3*.
- Buffered address, data, and control lines for off-board memory and I/O expansion; full DMA capabilities are provided by the buffer controllers.
- 3 MHz crystal-controlled clock.
- One 16-bit parallel I/O port, each bit individually programmable.

- Modified EIA RS-232-C serial I/O interface, capable of communication to both EIA-compatible terminals and popular modems (data sets).
- A local serial I/O port, with interfaces for an EIA terminal and either a teletype (TTY) or a twisted-pair balanced-line multi-drop system (interface choices are detailed in *Section 1.3*).
- Three programmable interval timers.
- Seventeen prioritized interrupts, including RESET and LOAD functions. Interrupt 6 is level triggered (active LOW) and edge-triggered (either polarity) and latched onboard.
- A directly addressable five-position DIP switch and an addressable LED for custom system applications.
- PROM memory decoders permit easy reassignment of memory map configuration; see *Figure 1-3* for memory map of the standard board.

The TM990/101MB is available in the three configurations specified in Table 1-1 below.

Table 1-1 TM990/101MB Configurations

TM990/101MB Dash No.	EPROM	RAM	Main Serial Port Option (EIA Terminal I/F Stand)
-1	Blank	2K x 16	TTY
-2	Blank	2K x 16	Multidrop
-3	2732A	2K x 16	TTY

1.5 GENERAL SPECIFICATIONS *(pages 1–5)*

Power Consumption:

	+5V		+12V		-12V	
	Typ	**Max**	**Typ**	**Max**	**Typ**	**Max**
TM990/101MB-1	1.0 A	2.2 A	0.20 A	0.4 A	0.10 A	0.4 A
TM990/101MB-2	1.0 A	2.2 A	0.20 A	0.4 A	0.10 A	0.4 A
TM990/101MB-3	1.1 A	2.6 A	0.25 A	0.5 A	0.10 A	0.5 A

Operating temperature: 0° to 70° C

NOTE

Operating temperature refers to ambient air temperature as measured within one inch of the component side of the module. The system designer must take into account enclosure temperature rises and unequal cooling (hot spot allowances) when designing a system for a given external environment.

Humidity: 0 to 95% noncondensing

Storage Temperature: –44° C to +85° C

Clock rate: 3 MHz

Baud rates (set by TIBUG monitor):
110, 300, 600, 1200, 2400, 4800, 9600, 19200

Memory Size: See Table 1-1

Board Dimensions: See *Figure 1-2*

Parallel I/O Port (P4): One 16-bit port, uses TMS 9901 programmable systems interface.

Serial I/O Port (P2 and P3): Two asynchronous ports:

Main port (P2) has two interfaces: RS-232-C answer mode and either a TTY or a balanced-line differential multi-drop interface.

Auxiliary port (P3) meets RS-232-C specification interface, capable of either originate or answer mode.

Both serial ports use TMS9902A asynchronous communication controllers, but the auxiliary port will readily accept the TMS9903 synchronous communication controller. Simply plug in the TMS9903 for synchronous systems.

2.4 POWER AND TERMINAL HOOKUP *(page 2-2)*

Check the board and verify that the jumper configuration is as described in Table 2-1 below.

Table 2-1 Board Jumper Positions (as shipped)

Function	Stake Pins Used	Proper Connection and Description
Interrupt 4 source	E1, E2, E3	E1 to E2 – pin 18, connector P1
Interrupt 5 source	E4, E5, E6	E4 to E5 – pin 17, connector P1
Slow EPROM	E7, E8, E53	E8 to E53 – No WAIT state
Map Select	E9 through E17	E9 to E10, E16 to E17, E13 to E14 – See Figure 6-8 Table B on page 6
EIA Connector Gnd	E18, E19	E18 to E19* – pin 1 of P3 grounded*
Microterminal +5V	E20, E21	Shipped installed on –1, 3 only*
Microterminal +12V	E22, E23	Shipped installed on –1, 3 only*
Microterminal –12V	E24, E25	Shipped installed on –1, 3 only*
Main EPROM type	E57 through E62	E57 to E58, E61 to E62 — 2732 type 4K x * EPROMs
Main RAM type	E73 through E78	E74 to E75, E77 to E78 — 6116 type 2K x 8 RAMs
Expansion sockets	E63 through E72	E66 to E67, E71 to E72 — 2732 type 4K x 8 EPROMs
Teletype	E36, E37	Shipped removed. On –1, 3 only. If using a TTY, borrow a micro terminal jumper plug for use here.
EIA/MD receive select	E38, E39, E40	E39 to E40 – EIA (and TTY) receive
multi-drop Terminal Resistors/Duplex	E41 through E52	Shipped installed on –2 only*
P3 Port Terminal/ Modem	E54, E55, E56	E54 to E55 – Terminal use*

*Jumper connection is not relevant for TIBUG operation with an RS-2342-C or TTY terminal.

6.9.1 Memory Address Decoding *(page 6-15)*

6.9.1.1 Memory Address Decoding PROM

The memory is programmed in a 74S287 PROM as shown in *Figure 6-8*. The PROM is a 256 x 4 bit memory, and each four-bit word (D04 to D01) is used to determine memory to be enabled. The most significant bit of the PROM word, D04, is the RAM enable control line. Setting the D04 bit to zero activates RAM.

The next bit of the PROM word (D03) can be programmed with a ZERO to enable the devices in U43 and U45. The distribution mapper PROM does not support devices at these locations.

EPROMs in U42 and U44 can be enabled by programming a ZERO in the next bit (D02).

The least significant bit of the PROM word (D01) is a negative-logic "OR" of the other three bits of the PROM word. If any of the other three bits are zero, this bit must be zero also. This signal indicates to data bus buffer control whether memory addressed is onboard or offboard; a zero state indicates onboard memory.

The memory address decoding PROM is enabled by MEMEN- when active low, and the lower five input bits are the most significant bits of the address bus (A0 to A4). The PROM selects memory in blocks of 1K words. The upper three address bits of the PROM have jumper options to choose the memory map preferred. There are eight address maps in the PROM controlled by the three jumpers. Each address map consists of 32 four-bit words, showing the state of each 1K word block in memory.

When MEMEN- is inactive, the PROM is disabled.

6.9.1.2 EPROM Selection

There are three basic memory maps for the EPROM: 2716s, 2732s, and 2764s. Each bank of memory actually consists of two devices, one for bits 0 to 7 of the addressed word, and the other for bits 8 to 15. Each EPROM bank is separate and can be programmed into any location by reprogramming the address decode PROM.

6.9.1.3 RAM Selection

RAM is decoded by D04 of the mapper PROM. The control signal DBIN will assert at the same time MEMEN- goes low during a read cycle, (see *Figure 6-10*) but WE- will not assert until after MEMEN- goes to zero on a write cycle.

PROM Address	MAP	PROM Output (48 bits each)
00	0	66FF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
20	1	66FF FFFF FFFF FFFF FFFF FFFF FFFF CCCC
40	2	FFFF FFFF FFFF FFFF FFFF FFFF FFFF FF66
60	3	CCCC FFFF FFFF FFFF FFFF FFFF FFFF FF66
80	4	66FF FFFF FFFF FFFF FFFF FFFF CCCC CCCC
A0	5	66FF FFFF FFFF FFFF FFFF FFFF FFFF FFCC
C0	6	CCCC CCCC FFFF FFFF FFFF FFFF FFFF FF66
E0	7	CCFF FFFF FFFF FFFF FFFF FFFF FFFF FF66

Figure 6-8 Table A. Mapper PROM Data

EPROM Used?	RAM Low or Hi	Read EPROM	Jumpers
MAP 0 = None	RAM Low	No EPROM	E10-E9,E16-E15,E13-E12
MAP 1 = 2732	RAM Low	Hi EPROM	E10-E9,E16-E15,E13-E14
MAP 2 = None	RAM Hi	No EPROM	E10-E9,E16-E17,E13-E12
MAP 3 = 2732	RAM Hi	Low EPROM	E10-E9,E16-E17,E13-E14
MAP 4 = 2764	RAM Low	Hi EPROM	E10-E11,E16-E15,E13-E12
MAP 5 = 2716	RAM Low	Hi EPROM	E10-E11,E16-E15,E13-E14
MAP 6 = 2764	RAM Hi	Low EPROM	E10-E11,E16-E17,E13-E12
MAP 7 = 2716	RAM Hi	Low EPROM	E10-E11,E16-E17,E13-E14

NOTE

The mapper ROM supplied with the TM990/101MB board requires that ROMs be installed in U42/U44 and RAMs in U30/U31. Devices installed in U43/U45 are not supported.

Figure 6-8 Table B. TM990/101MB Map Configuration (set by jumpers)

6.11 READ ONLY MEMORY *(page 6-27)*

Two 28-pin sockets (U42 and U44) are provided to use 2716, 2732, and 2764 single voltage EPROMs. Reprogramming the mapper PROM (U19) allows the use of 27128 EPROMs. Jumper options at E57 through E62 select the EPROM type used. Figure 6-11 shows the EPROM array.

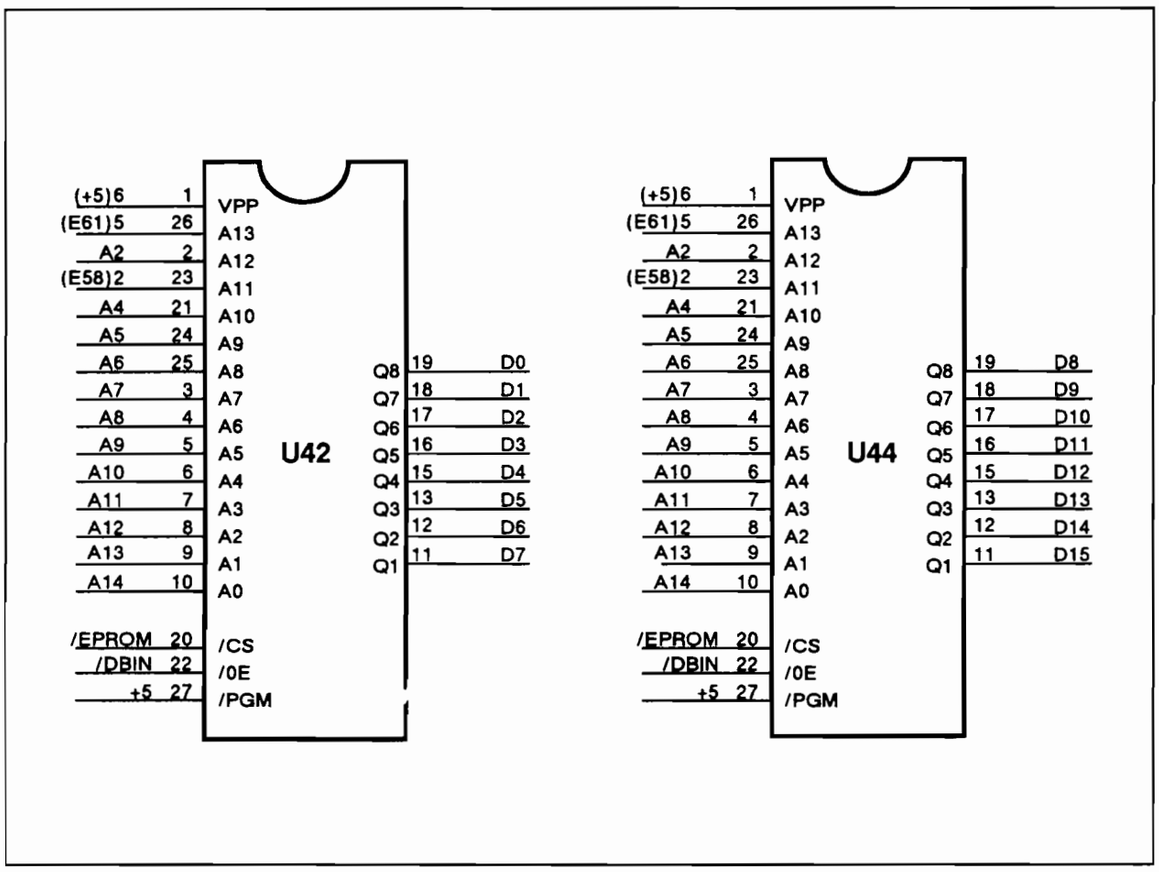

Figure 6-11 Read-Only Memory

NOTE

The EPROM array in Figure 6-11 shows data lines D0 - D7 (U42) and D8 - D15 (U44) for 101MB boards. For 101MB boards, the data lines are switched. D0 - D7 are on U44 and D8 - D15 are on U42, which swaps the LSB and MSB positions.

6.12 RANDOM ACCESS MEMORY *(page 6-28)*

The standard TM990/101MB is populated with 2K words of RAM (two HM6116s) in U30 and U31. The 2K x 8 devices may be replaced with optional 8K x 8 devices (HM6264s)—this requires changing the mapper PROM. Figure 6-12 shows the RAM array.

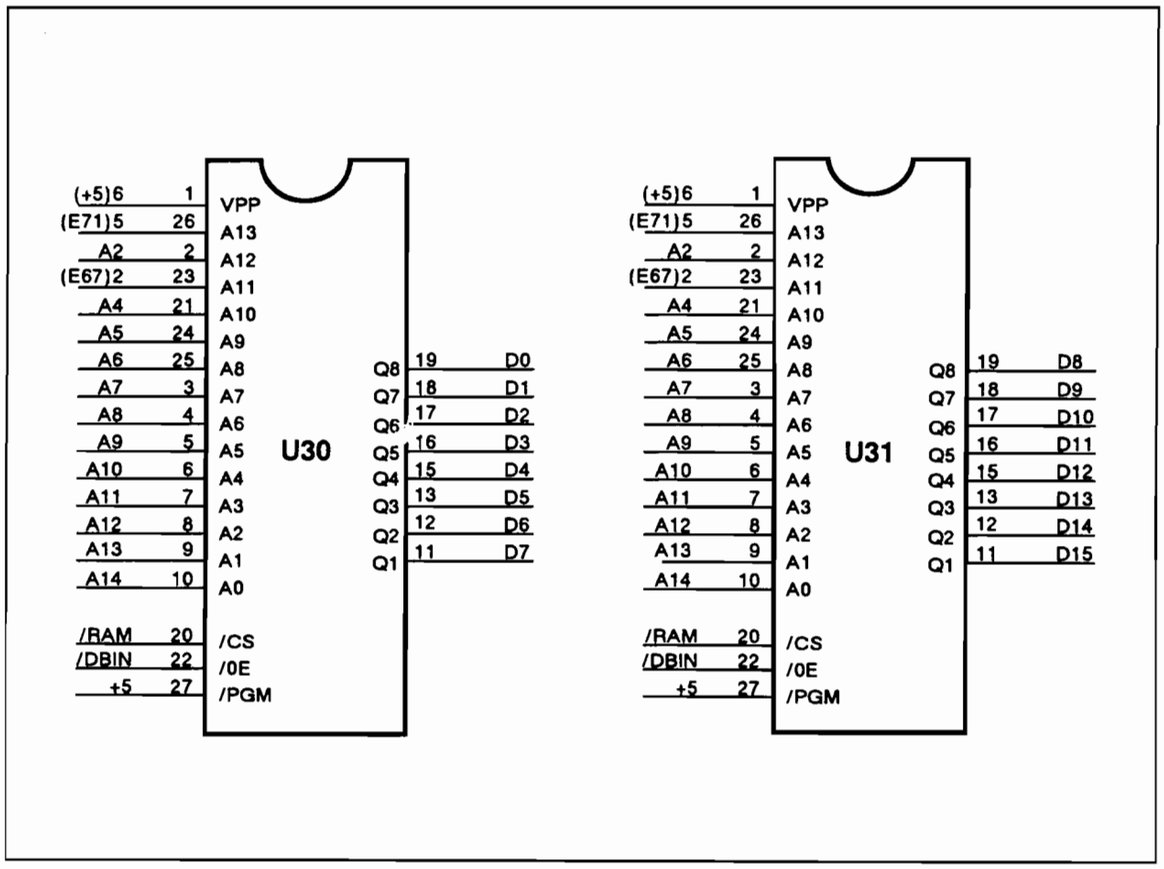

Figure 6-12 Random Access Memory

7.1 GENERAL *(page 7-1)*

Options available with the TM990/101MB include:

- Use of 2716, 2732, 2764, 27128 single voltage EPROMs
- On-card expansion of EPROM and RAM
- Asynchronous serial interrupt from TMS 9902
- RS-232-C/TTY/multi-drop interfaces with the Local Serial Port
- External switch actuation of a RESET or RESTART signal
- Memory chip and CRU device selected by bit masks in PROMs
- Line-by-line Assembler in EPROM
- TM990/301 microterminal use

Table 7-1 is a summary of jumpers and capacitors used with the options. Figure 7-1 shows board locations applicable to this section.

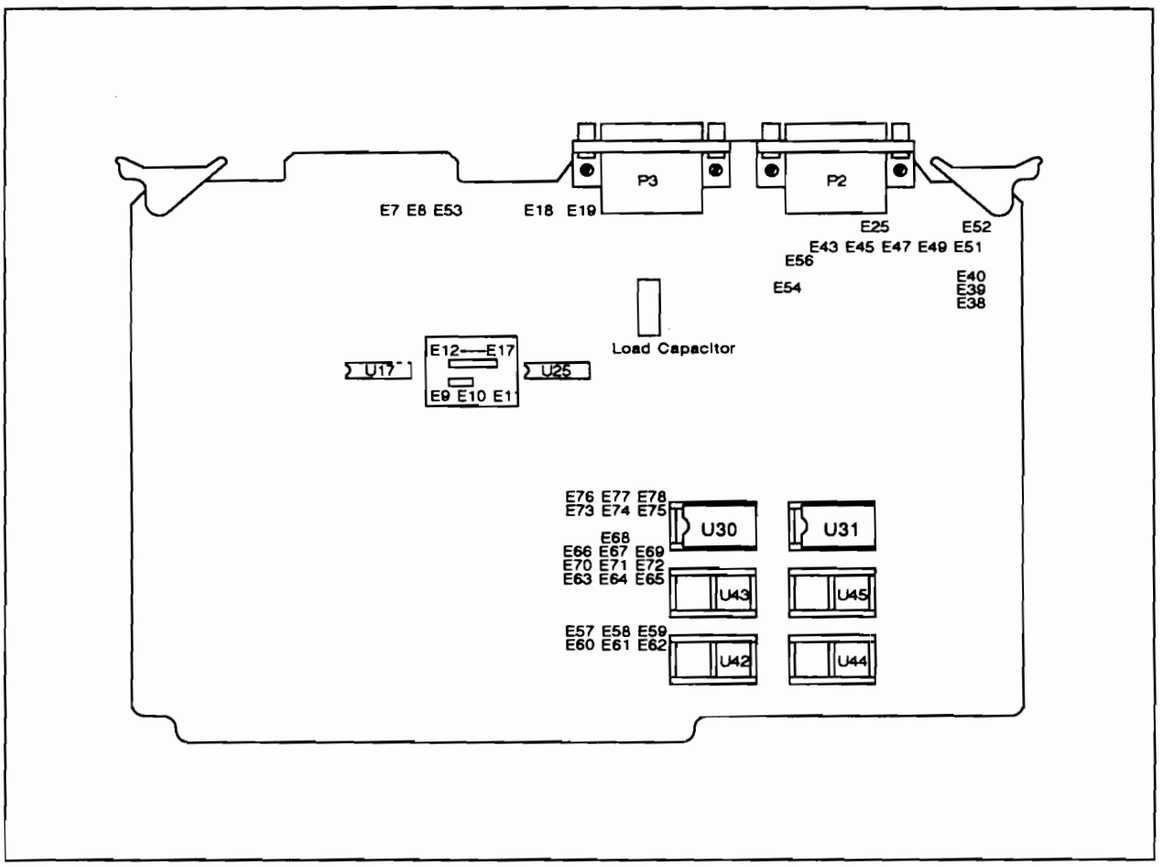

Figure 7-1 Jumper Placement

7.2 ONBOARD MEMORY EXPANSION *(page 7-1)*

7.2.1 EPROM Expansion

EPROM memory can be expanded by using different device types (2716, 2732, or 2764) installed in U42 and U44 (see Figure 7-1). Using 27128 EPROMs requires a new memory mapper PROM.

Refer to Figure 6-8 Table B for the memory maps available with the standard distribution mapper PROM. Refer to Figure 7-3 Table A for the jumper patterns for the different device types that can be used in the TM990/101MB memory.

	U42/U44	U43/U45	U30/U31
2716	E58–E59 E61–E62	E67–E69 E71–E72	—
2732	E57–E58 E61–E62	E66–E67 E71–E72	—
2764	E57–E58 E60–E61	E63–E64 E66–E67 E70–E71	—
27128	E57–E58 E60–E61	E63–E64 E66–E67 E70–E71	—
2K X 8 RAM	—	E67–E68 E71–E72	E74–E75 E77–E78
8K X 8 RAM	—	E71–E72 E66–E67 E63–E64	E73–E74 E77–E78

Figure 7-3 Table A. TM990/101MB Memory Type Jumpers

7.2.2 RAM Expansion

RAM memory can be expanded by replacing the 2K x 8 (HM6116) devices with 8K x 8 (HM6264) devices and changing the mapper PROM.

RAM may also be expanded by populating U43 and U45 with random access memory.

7.8 MEMORY MAP CHANGE *(page 7-12)*

Onboard memory chip and CRU device addressing is through bit patterns in two PROMs, a 74S287 and 74S288 as shown in the enclosed schematics.

This memory map may be altered by the substitution of PROMs with the preferred configuration. Refer to Figure 6-8 Table A for the PROM bit pattern in the distribution memory mapper device.

RMR Card

If you should have a problem with this product and need to return it to Texas Instruments, please remove this page, fill in the requested information and send it with the product to the following address.

Texas Instruments
3000 Bill Garland Road
Johnson City, TN 37601

Customer Problem Tag

If service is required on this device, please call

1-800-284-9084 (outside Tennessee)

1-615-461-2500 (inside Tennessee)

for the location of your nearest distributor.

Customer Name _____

Company Name _____

Phone Number _____

RMR Number _____

Part Number _____

Serial Number _____

In the event of failure, to help expedite repair and prompt return of device, please describe the symptom(s) and configuration in which the failure occurred.

Problem: _____

_____

_____

_____

_____

_____

_____

_____

_____