

TM990/BUS

T-BUS MICROCOMPUTERS

FEATURES:

- Provides a standard electrical and mechanical connection.
- Flexibility provides a wide range of configurations.
- Easy to interface from custom boards.
- CRU interfacing.
- DMA capability.
- 20 bit address bus allows up to 1M Byte addressing capability.
- 28 lines for power and ground.
- 20 lines for address bus.
- 16 lines for the data bus.
- 18 lines for bus control.
- 15 lines for prioritised interrupts.
- 3 lines for CRU interfacing.

DESCRIPTION:

Power Bus:- 4 lines for +5V, 2 lines for +12V, 2 lines -12V, 2 lines for battery voltage, 2 lines for auxillary voltage and 16 lines for ground.

Address Bus:- 16 lines of basic address space, 4 lines of extended addressing giving 1MByte memory address range. Can address CRU locations, and is controlled by the bus master, the bus isn't terminated on the back plane.

Data Bus:- 16 lines for data, used to transfer data between processors, memory and peripherals. It is controlled by the current bus master and is not terminated on the back plane.

CRU Bus:- Used for serial data transfer, 3 lines provide separate information paths, CRUIN serial input line, CRUOUT serial output line, CRUCLK clock signal gating data.

Interrupt Bus:- Fifteen lines allows each level of prioritized interrupts.

Control Bus:- 15 separate lines to control data transfers and system synch 4 memory control signals MEMEN, MEMCYC, DBIN and READY which indicate bus contains a valid memory address, memory cycle in progress, data bus inputting data and memory will be ready to complete its memory access, respectively.

2 timing and sync signals, BUSCLK and REFCLK, both generated by the master processor to cause sync of memory and bus cycles and timing reference to I/O devices respectively.

5 bus arbitration signals HOLD, HOLDA, BUSY, GRANTIN, GRANTOUT. Which indicate a device is requesting the bus for data transfer, bus master has relinquished control of the bus to the requesting device, requesting device has taken bus, no device with higher priority is requesting the bus, and that a lower priority device may request control of the bus, respectively. GRANTIN and GRANTOUT form a daisy chain priority scheme for transferring bus control.

4 miscellaneous signals:- IORST, PRES, RESTART, IAQ, which indicate to the system that a system reset is in progress to the I/O devices, power supply has stabilised and processor can begin execution, a load function should be performed and an instruction fetch is being performed by the processor respectively.

TM990 SYSTEM BUS PIN DEFINITION

PIN	SIGNAL	GROUP	PIN	SIGNAL	GROUP
1	GND	Power/Ground	2	GND	Power/Ground
3	+5V		4	+5V	
5	INT8		6	INT7	
7	INT10		8	INT9	
9	INT12		10	INT11	
11	INT14	Interrupt	12	INT13	Interrupt
13	INT2		14	INT15	
15	INT3		16	INT1	
17	INT5		18	INT4	
19	IAQ	Control Bus	20	INT6	
21	GND		22	BUSCLK	
23	GND		24	REFCLK	
25	GND	Power/Ground	26	RESERVED	
27	GND		28	RESERVED	
29	CRUIN		30	CRUOUT	CRU Bus
31	GND		32	BUSY	Control Bus
33	D0		34	D1	
35	D2		36	D3	
37	D4		38	D5	
39	D6	Data Bus	40	D7	Data Bus
41	D8		42	D9	
43	D10		44	D11	
45	D12		46	D13	
47	D14		48	D15	
49	VAUX		50	VAUX	Power/Ground
51	VBATT	Power/Ground	52	VBATT	
53	XA0		54	XA1	
55	XA2		56	XA3	
57	A0		58	A1	
59	A2		60	A3	
61	A4		62	A5	
63	A6	Address Bus	64	A7	Address Bus
65	A8		66	A9	
67	A10		68	A11	
69	A12		70	A13	
71	A14		72	A15	
73	-12V		74	-12V	Power/Ground
75	+12V		76	+12V	
77	GND	Power/Ground	78	WE	
79	GND		80	MEMEN	
81	GND		82	DBIN	← not in vokat.
83	GND		84	MEMCYC	
85	GND		86	HOLDA	
87	CRUCLK	CRU Bus	88	IORST	Control Bus
89	GND		90	READY	
91	GND	Power/Ground	92	HOLD	
93	RESTART	Control Bus	94	PRES	
95	GRANTOUT		96	GRANTIN	
97	+5V	Power/Ground	98	+5V	Power/Ground
99	GND		100	GND	