T.I. TM-990/100M Compatible Analog I/O Subsystems

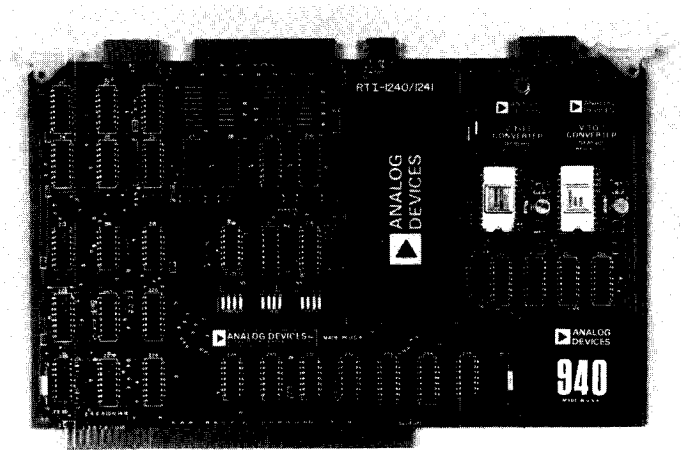
MODELS RTI-1240, 1241, 1242, 1243

FEATURES
- **Complete Analog I/O Subsystems**
- **T.I. 16 Bit TM-990/100M Compatibility**
- **Memory Mapped I/O Interface**
- **12 Bit Resolution and Accuracy**
- **Optional Single +5V Power**
- **Wire Wrap Feature Selection**

INPUT SUBSYSTEMS
- **256 Channel Expansion Capability**
- **Input Overvoltage Protection**
- **Software or Resistor Programmable Gain**
- **Interrupt Operation Capability**
- **Optional Analog Output Channels**

OUTPUT SUBSYSTEMS
- **8 High Current Logic Driver Outputs**
- **4 or 8 Analog Output Channels**

- **Detailed User's Guide**



SERIES DESCRIPTION

The RTI-1240 Series are complete, 12 bit resolution, analog I/O subsystems which are electrically and mechanically compatible with the Texas Instruments 16 bit TM-990/100M single board microcomputer. The series is comprised of an input only board, an output only board, and a combination I/O board; each of which interfaces to the microcomputer as a block of 8 or 16 address locations (memory mapped interface). All data bus, control bus and address bus connections to the microcomputer are made by simply plugging the board into the computer card cage. The analog signals connect at the opposite board edge from the digital bus connector.

Many additional capabilities, features and options are included to reduce both the hardware and the software effort required in interfacing analog signals to the microcomputer. The designer is then free to spend more time and effort on the particular application instead of on designing basic building block functions.

RTI-1240 ANALOG INPUT SUBSYSTEM —

GENERAL DESCRIPTION

The basic function of the RTI-1240 is to acquire signals and present them to the microcomputer in digital form. The design is comprised of a protected input multiplexer, either a resistor or a software programmble gain instrumentation amplifier, a sample and hold amplifier, a 12 bit A/D converter and the associated digital interface logic as shown in the block diagram.

INPUT MULTIPLEXER

The RTI-1240 is available with up to 32 single-ended/16 differential protected input channels on-board, and has the capability of off-board expansion to 256 channels using on-board control logic. The multiplexer (MUX) channel can be randomly selected at the MUX word in the memory map as shown further. The MUX can also be incremented to the next channel upon receipt of a convert command. This auto increment feature is enabled by a software command to the setup word which allows scanning and random channel addressing to be mixed under software control.

INSTRUMENTATION AMPLIFIER/SAMPLE AND HOLD AMPLIFIER

The RTI-1240 is available with two types of instrumentation amplifiers (IA) which provide 12 bit compatible CMRR and CMV specifications. The software-programmable-gain (1-2-4-8) IA provides dynamic range expansion through subranging as well as the flexibility of using different gain settings for each input channel to accommodate different signal levels. The resistor-programmable gain IA may be used for input ranges from 10mV F.S. to ±10V F.S. There is very little loss of speed and no degradation of linearity at high gains.

The sample and hold amplifier (SHA) allows sampling of high slew rate signals and is automatically switched to the hold mode upon receipt of a convert command. The RTI-1240 also has a built-in provision which delays the convert command to allow for input section settling following a gain change or channel change. For very high gain applications, the convert command delay can be increased either through software or by addition of a single resistor.

SPECIFICATIONS (typical @ +25°C and nominal supply voltage)

ANALOG INPUT	COMBINATION I/O BOARDS		INPUT ONLY BOARDS	
Model Numbers	RTI-1241-R	RTI-1241-S	RTI-1240-R	RTI-1240-S
Input Channels				
Basic Board	16 SE, 16 PD, 8 Diff.[1]	*	*	*
Expansion: On-Board	32 SE, 32 PD, 16 Diff.[1]	*	*	*
Off-Board	256 Total	*	*	*
Input Range at Card Edge[2]	10mVFS to ±10VFS	0.625 to ±10VFS	*	**
Current Loop Inputs[3]	0 to 50mA, 0 to 20mA, etc.	*	*	*
Input Protection	$\pm(V_{CC}$ +20V)	*	*	*
Switching	Break-Before-Make	*	*	*
Input Impedance	$>10^8\Omega$	*	*	*
Input Bias Current	±50nA max	±5nA max	*	**
0 to +70°C	±70nA	±50nA	*	**
Instrumentation Amplifier	Resistor Programmable Gain	Software Programmable Gain	*	**
Gain Range	1 to 1000 V/V	1, 2, 4, 8 V/V	*	**
CMV	±10V min	*	*	*
CMRR (dc–500Hz)	76dB min	*	*	*
Input Settling Time[4]	15μs max (G = 1)	10μs max (G = 1 to 8)	*	**
ADC Input Ranges[1]	±5V, ±5.12V, ±10V, ±10.24V, +10V, +10.24V	*	*	*
Resolution	12 Bits	*	*	*
Conversion Time	25μs max	*	*	*
Throughput Rate[5]	40,000 Channels/sec	*	*	*
Output Codes[1]	Binary, Offset Binary, Two's Complement	*	*	*
Nonlinearity Error	±1/2LSB typ (±1LSB max)	*	*	*
Offset Error[6]	Adj. to Zero	*	*	**
Gain Error[6]	Adj. to Zero	*	*	*
Offset TC	$\pm(1 + \frac{20}{G})\mu V/^\circ C$ (RTI)	±30μV/°C (RTI)	*	**
Gain TC	±20ppm of rdg/°C (RTI)	±25ppm of rdg/°C (RTI)	*	**
Noise Error[7]	±1/4LSB max	*	*	*
Overall Error @ G = 1[8]	±1LSB max	*	*	*
SHA Aperture Delay	90ns	*	*	*
SHA Aperture Width	20ns	*	*	*
SHA Aperture Uncertainty	5ns	*	*	*

ANALOG OUTPUT	OUTPUT ONLY BOARDS			
Model Number	RTI-1241-R	RTI-1241-S	RTI-1242	RTI-1243
Output Channels	2	2	4	8
Resolution	12 Bits	*	*	*
Output Ranges[1] (with on board Ref)	+5V, +10V, ±2.5V, +5V, +10V	*	*	*
Output Current	±5mA min @ ±10V	*	*	*
Nonlinearity Error @ +10V Ref	±0.01% max	*	*	*
Offset Error	Adj. to Zero	*	*	*
Gain Error	Adj. to Zero	*	*	*
Offset TC	±15μV/°C	*	*	*
Gain TC	±15ppm/°C	*	*	*
Settling Time[8] (for 20V step to ±0.01%)	10μs	*	*	*
Reference Range External[9]	1V to +10V	*	*	*
Input Codes	Binary, Two's Complement, or Offset Binary	*	*	*
OTHER OUTPUTS	2 Optional Current Loops	*	8 Logic Drivers	***
Type	ISA-S50.1, Type 3, Class 6	*	Open Collector	***
Output Current Range[10]	4-20mA	*	300mA sink @ 0.7V	***
Supply Voltage Range	+15V to +30V	*	+30V max	***
Input Voltage Range	0V to +10V	*		
Offset Error	Adj. to Zero	*		
Gain Error	Adj. to Zero	*		
Offset TC	±0.4μA/°C	*		
Gain TC	±30ppm/°C	*		
Nonlinearity Error	±0.01% max	*		
Settling Time	50μs max to 0.02%	*		

POWER REQUIREMENTS

Model Number	RTI-1240	RTI-1241	RTI-1242	RTI-1243	V/I
Without Optional dc-dc					
+15V ±3%	40mA	50mA	45mA	50mA	10mA
−15V ±3%	40mA	80mA	80mA	150mA	2mA
+5V ±5%	1100mA	1100mA	900mA	1000mA	0mA
With dc-dc Option					
+5V ±5%	1.4A	1.5A	1.3A	1.6A	mA

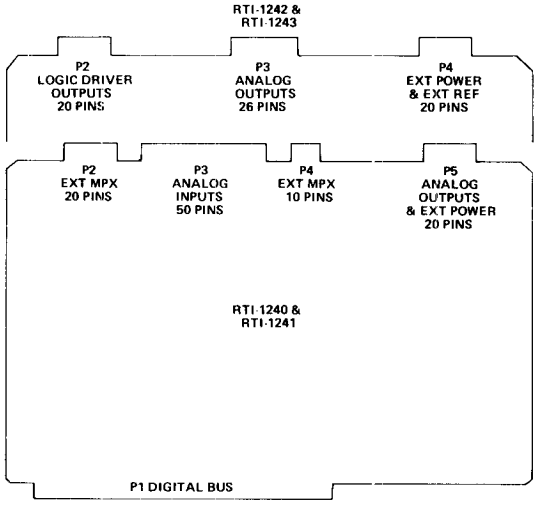
MECHANICAL (All Models)

Size	7.5" x 11.0" (190.5mm x 279.4mm)
Card Outline	Conforms to Texas Instruments Drawing SK922321
Card Spacing	0.6" min (15.2mm)

*Same as for RTI-1241-R
**Same as for RTI-1241-S
***Same as for RTI-1242
Specifications subject to change without notice.

NOTES
[1] User selectable by wire wrap jumpers.
[2] The full scale input signal range is the A/D converter range divided by the gain of the instrumentation amplifier.
[3] The user may install one resistor per channel (SE or Diff) to convert the input current to the proper voltage range. Any input current span can therefore be accommodated.
[4] Input settling time applies to either a multiplexer channel change or a software controlled gain change. The settling time increases to 50μs @ G = 1000.
[5] The effective throughput rate is determined by the user's software data handling capability. The max throughput rate listed is exclusive of the CPU interface operations which may or may not be completed during the subsystem's conversion time. In CPU hold mode, the user's software and interface time obviously must be added to the conversion time to determine the maximum effective throughput rate.
[6] For any one programmable gain setting. Maximum offset shift of ±1LSB or gain shift of ±0.02% when using a programmable gain setting other than the one used during calibration.
[7] Noise error increases to ±1/2LSB max @ G = 8 for the SPG models and to ±1LSB @ G = 100 for the RPG models.
[8] Overall error increased to ±2LSB max @ G = 8 for the SPG models and 2LSB max @ G = 1000 for the RPG models.
[9] Overall error increases to 0.1% @ 1V external reference.
[10] The current loop load resistance range is 0Ω to 450Ω with a +15V supply. A load resistance of 500Ω may be used with a +18V supply.

MECHANICAL OUTLINE AND CONNECTOR DIAGRAM



ORDERING GUIDE

MODEL NUMBER	DESCRIPTION
RTI-1240-R	Input Board with Resistor Programmable Gain Amplifier
RTI-1240-S	Input Board with Software PGA
RTI-1241-R	I/O Board with Resistor PGA
RTI-1241-S	I/O Board with Software PGA
RTI-1242	Output Board with Four DACs
RTI-1243	Output Board with Eight DACs
ACCESSORIES	
0A08	4-20mA V/I Module
0A09	DC-DC Converter
0A10	Multiplexer Expansion Kit (2 ea. HI-508A)
CONNECTORS	
AC1556	20 pin, Card Edge*
AC1557	50 pin, Card Edge*
AC1558	10 pin, Card Edge*
AC1559	26 pin, Card Edge*

*ALL CONNECTORS HAVE 3' OF COLOR CODED CABLE ATTACHED

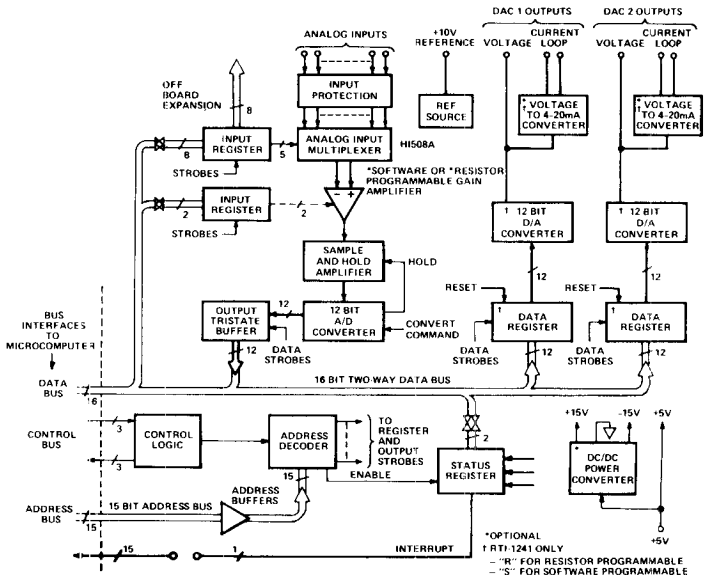


Figure 1. RTI-1240 & RTI-1241 Functional Block Diagram

ANALOG/DIGITAL CONVERTER

The RTI-1240 provides the user the choice of selecting either single instruction programming for software simplicity or variations of polled status programming for the highest data throughput rates.

The RTI-1240 contains a fast, 12 bit, successive approximation converter. The user can select one of six ADC input ranges and one of three output codes with wire-wrap jumpers.

The subsystem can be used in any of three operation modes:

1. The *CPU Hold Mode* allows the user to initiate conversions and read or operate upon ADC data with a single instruction. This results in the simplest software programs for acquisition of data.
2. In the *Interrupt Mode*, the setting of the end of conversion bit in the status word can be made to create a CPU interrupt. Reading the status word clears both the EOC bit and the associated interrupt, and is the only acknowledgement required. This results in very efficient polling.
3. In the normal *Polled Status Mode*, the CPU reads the EOC bit in the status word to determine if the ADC data is valid. This allows the most software flexibility and can be mixed with the software controlled EOC Interrupt Mode for truly versatile data acquisition system operation.

MICROCOMPUTER INTERFACE

The digital hardware interface to the microcomputer is made through the T.I. 100 pin digital bus. Each board's base address is selected at the on-board address sockets while the least significant bits of any memory reference instruction address determine which word is addressed in the memory maps (shown further).

The optional status words allow the user some flexibility during polling to read either ADC data or gain and multiplexer data at the same time that the status word is read. An under-range bit for gain ranging applications is available in the status word to indicate when the signal just converted is small enough to permit a higher gain and that a higher gain is still available.

Several timing and control signal lines are available at the board edge for signal and converter synchronization (converter status, external convert command, internal convert commands and the convert command delay gate). With software control over the EOC Interrupt, External Convert Command, and Auto Increment features, and with the converter signals readily available, the user has complete control over the analog input function.

POWER SUPPLY

In addition to the +5V logic power required for the digital interface circuits, the RTI-1240 series require ±15V power for its analog circuitry. These voltages can be supplied by the user at a card edge connector or the ±15V can be supplied from an optional card mounted dc-dc converter (P/N0A09).

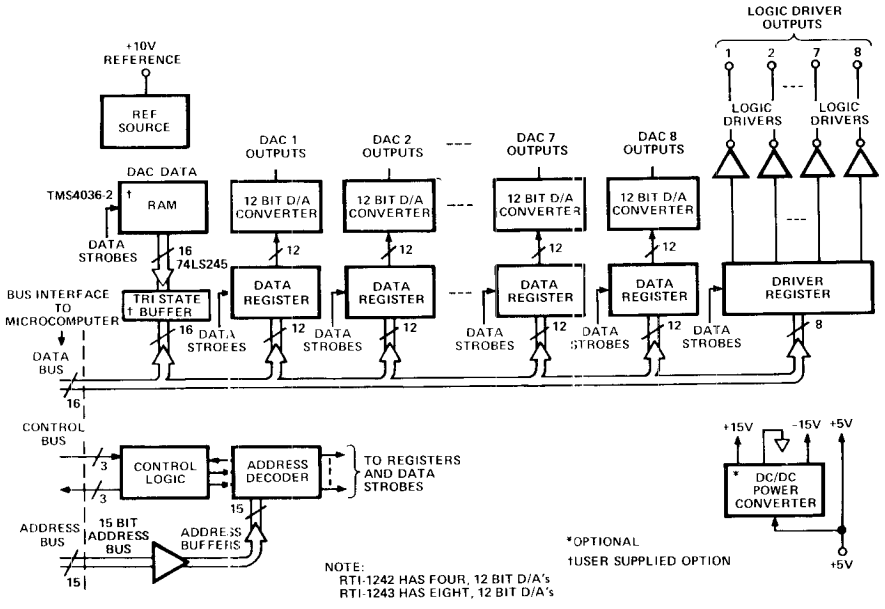


Figure 2. RTI-1242 & RTI-1243 Functional Block Diagram

RTI-1241 COMBINATION ANALOG I/O INTERFACE

The RTI-1241 provides the same analog input functions as the RTI-1240 and in addition has two channels of 12 bit analog output.

ANALOG OUTPUTS

The RTI-1241 has two 12 bit resolution D/A converters (DAC's) providing up to ±10V analog output in several ranges. The input coding and output range of each DAC are independently selectable by wire-wrap jumpers.

REFERENCE

The +10V reference for the DAC's is located on-board. However, should the user desire, an external reference between +1V and +10V may be used.

RESET

By installing optional jumpers, the DAC's will reset to zero volts upon system reset. This feature can be used to reduce output transients when system power is applied.

CURRENT LOOP OUTPUTS

The two analog output channels can also be ordered with optional 4-20mA current loop outputs for use in process and industrial control applications. These voltage to current (V/I) converter modules (P/N 0A08) meet all the requirements of ISA-S50.1 for Type 3, Class L, non-isolated 4-20mA current loop transmitters.

RTI-1242 AND RTI-1243 OUTPUT SUBSYSTEMS

The RTI-1242 and 1243 output subsystems provide 4 or 8 channels of analog output and 8 high current, logic driver outputs. The block diagram above shows the basic output functions and optional features.

LOGIC OUTPUTS

The eight digital outputs are software controlled, open collector, drivers capable of 300mA maximum sink current and voltages up to +30V. They can be used to provide "on/off" system functions for relay, solenoid, and valve control.

ANALOG OUTPUTS

The RTI-1242 and RTI-1243 have four or eight 12 bit DAC's respectively. Each DAC's input code and output range is independently selectable.

REFERENCE

The RTI-1242 and RTI-1243 each have a single on-board +10V precision reference to provide excellent tracking between channels. Each board also provides inputs for external references. The user can select an external reference between +1V and +10V to provide tracking between several boards or for scaling or multiplying functions.

REMOTE LOAD SENSING

Each DAC has an external load sensing capability for applications where the load is to be located a considerable distance from the DAC output. Without this feature, IR voltage losses in the output line could degrade overall accuracy.

READBACK

Both output subsystems provide sockets for RAM's and buffers (T.I. P/N TMS4036-2 and 74LS245) to allow DAC and driver data to be read back to the microcomputer. This feature offers additional software flexibility and convenience since it eliminates the need for scratch pad memory or software overhead to store data written to the RTI-1242 or RTI-1243 DAC's and drivers.

RESET

When enabled by wire-wrap jumpers, the DAC's and/or logic drivers, will reset upon occurrence of a system reset. The DAC's will reset to 0V and the logic drivers reset to the "off" (High level) state. This feature will allow the system to start from a known state after initially applying power to the system or after a momentary loss of power.

INPUT BOARD MEMORY INTERFACE
RTI-1240 AND RTI-1241

The RTI-1240 and RTI-1241 have the same basic memory image format. The sole difference is that the RTI-1241 I/O board had two DAC words corresponding to the two on-board DAC's. These two addresses are not used on the RTI-1240.

BASE ADDRESS SELECTION

The RTI-1240 and RTI-1241 subsystems occupy 8 consecutive 16 bit word addresses. To determine the most significant hexadecimal digits of the base address, the user installs switches or shorting plugs at three on-board sockets.

DAC DATA WORDS (BASE + 0 AND + 2, RTI-1241 ONLY)

DAC outputs are set by writing the digital data to the corresponding DAC address. Data can be in either binary, offset binary or two's complement coding.

SETUP WORD (BASE + 4)

By loading the three most significant bits of the setup word, any of three software controlled features may be enabled. The MSB is the End of Conversion (EOC) Interrupt enable bit. By enabling this feature the EOC signal from the ADC will create an interrupt on the interrupt line previously selected by a wire wrap jumper. When bit 2 is set, the multiplexer will increment to the next sequential channel just after the SHA holds for each conversion in the Auto Scan Mode. Writing a one to bit 3 enables external convert command signals to be applied to the converter. These three software enabled features allow the user flexibility in creating system software for each particular application.

GAIN WORD (BASE + 6, "S" MODELS ONLY)

By writing the appropriate code into this word, the gain of the software programmable instrumentation amplifier is set. Auto-gain-ranging for a dynamic range of 15 bits is possible through the use of this feature.

MULTIPLEXER CHANNEL WORD (BASE + 8)

Any random input channel can be selected by writing the channel address code into this word. The beginning channel of a scan using the auto-scan feature is also selected in this manner. Up to 256 channels can be addressed at this location using on-board logic.

CONVERT COMMAND WORD (BASE + A)

By writing any data into this word a convert command is issued to the ADC. This is the standard mode of operation but other means of creating this command exists. Externally generated convert commands can be connected via the P-2 edge connector. Convert commands can also be generated by ADC data read instructions in CPU Hold Mode operation.

STATUS WORD (BASE + C)

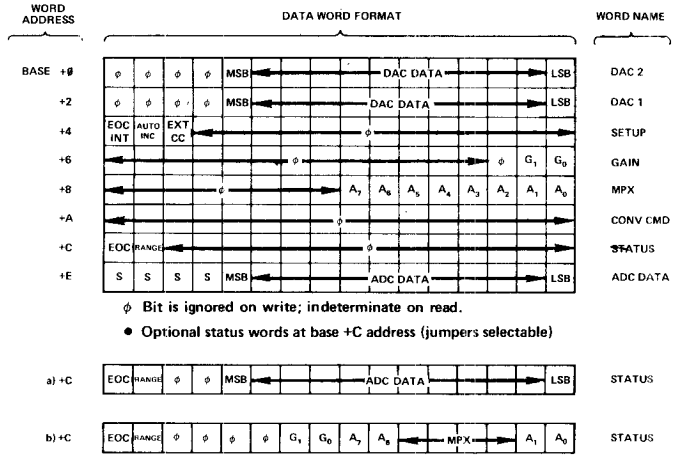
The end of conversion (EOC) bit in the status word is set when the conversion is complete. Reading the status word resets the EOC bit and any associated interrupt.

The status word also contains an underrange bit for gain ranging applications on models equipped with a software programmable gain amplifier. This bit is set whenever a higher gain range is still available and when the signal being measured is small enough to permit the use of a higher gain.

Additional information can be provided in the status word by selecting wire-wrap jumpers. Gain and MUX channel data are made available with one jumper and the ADC data is available with the other jumper selection. These status word variations allow very efficient programs and high operating speeds.

ADC DATA WORD (BASE + E)

ADC data is available at this address (and, if enabled by jumper option, in the status word). It remains valid until the next conversion begins. When using two's complement code and a bipolar input range, the most significant four bits of the ADC Data word are sign extension bits.



RTI-1240, 1241 Address Map

SAMPLE PROGRAM FOR NORMAL MODE

```
NXT   SETO  *R1     Send conv. comm.        ]
      INCT   R2     Update data store addr. |
      DEC    R3 ]   Decr. sample counter    |  Conv.
      JLE    OUT ]  Out if done             |  in
CK    INV   *R5 ]   Status (Data Ready)     |  Process
      JLT    CK  ]  Check Loop              |
      MOV   *R4,*R2 Store Data Sample       |
      JMP    NXT    Next Sample             ]
OUT
```

This program takes N samples on one channel and stores them in successive memory locations.

Registers: R1 – Conv. Comm. Address
R2 – Data Storage Address Pointer
R3 – Sample Counter: Initialize to No. of Samples
R4 – ADC Data Address
R5 – Status Word Address

SAMPLE PROGRAM FOR WAIT MODE

```
NXT   MOV   *R4,*R2 + ]  Start Conversion; Read Resulting
                      |  Data; Store in Memory; Update
                      ]  Data Store Address
      DEC    R3        Decr. Sample Counter
      JH     NXT       Out if Done. Otherwise Next Sample
```

This program does the same job as the Normal Mode example above. In this case, but not in general, the speed is about the same.

OUTPUT BOARD MEMORY INTERFACE

BASE ADDRESS SELECTION

This is set in the same manner as for the RTI-1240 and RTI-1241 as shown on the previous page.

DRIVER DATA WORD (BASE + 10)

The logic drivers may be turned "on" (to sink up to 300mA of current) by writing ones at the appropriate driver data bits in the driver data word. When turned "off" by writing a zero to the corresponding bit each driver takes up to +30V at the collector. The logic drivers are capable of being reset to the "off" condition upon system reset by connecting a wire wrap jumper.

DAC DATA WORDS (BASE + 1A THROUGH 1E)

As with the RTI-1241 each DAC receives update information from the data written into the corresponding DAC data word. By wire wrap jumper the output subsystem DAC's may also be reset to 0 volts output upon receipt of a system reset.

OPTIONAL MEMORY IMAGES

If the logic drivers are not used, the user may select an optional address map for the RTI-1243 with only 8 words. Another 8 word address map is available for use with the RTI-1242.

SAMPLE PROGRAM FOR ANALOG OUTPUTS

```
NXT   MOV   *R2+, *R6
      DEC   R3
      JLE   OUT
      JMP   NXT
```

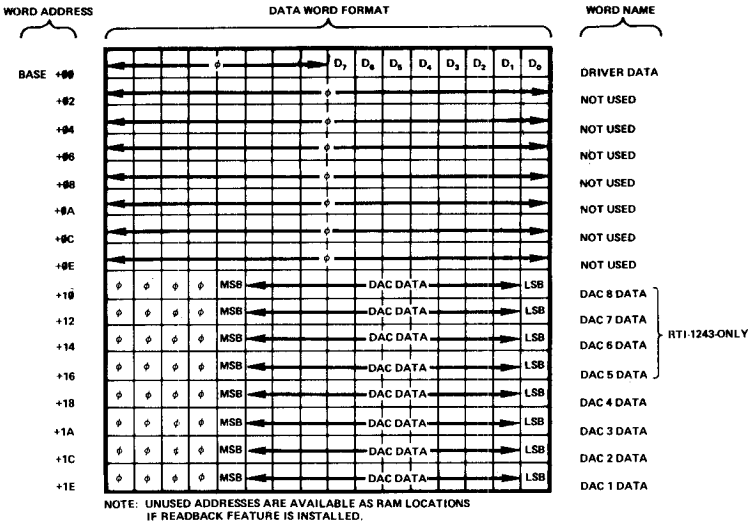
This program outputs a set of samples stored in memory to the DAC channel whose address is stored in R6. Transfer rate is approximately 1 sample/17 microseconds. If desired, a delay loop can be inserted to permit a slower update rate

Register usage:

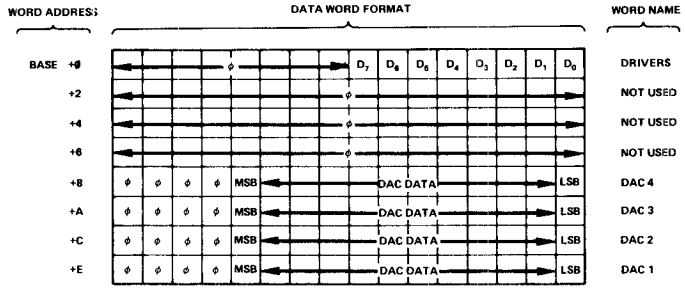
- R2: Memory address of data block
- R3: Sample counter
- R6: Address of DAC in use

DETAILED USER'S MANUAL

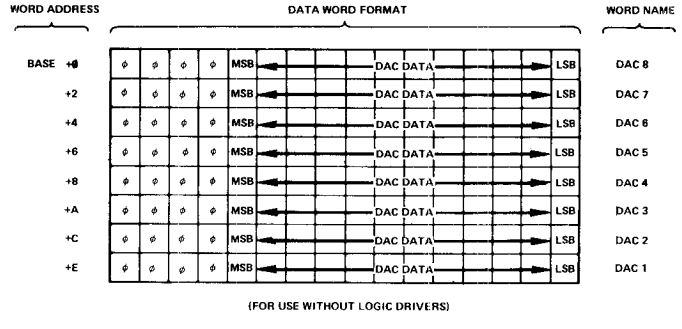
A detailed manual giving installation and operation instructions along with suggested software routines for calibration and operation is provided with each RTI-Subsystem. This manual also provides theory of operation as well as schematics and tables to enable the user to install, and start operating the system as easily and quickly as possible.



Standard RTI-1242 & RTI-1243 Address Map



Optional RTI-1242 Address Map



Optional RTI-1243 Address Map