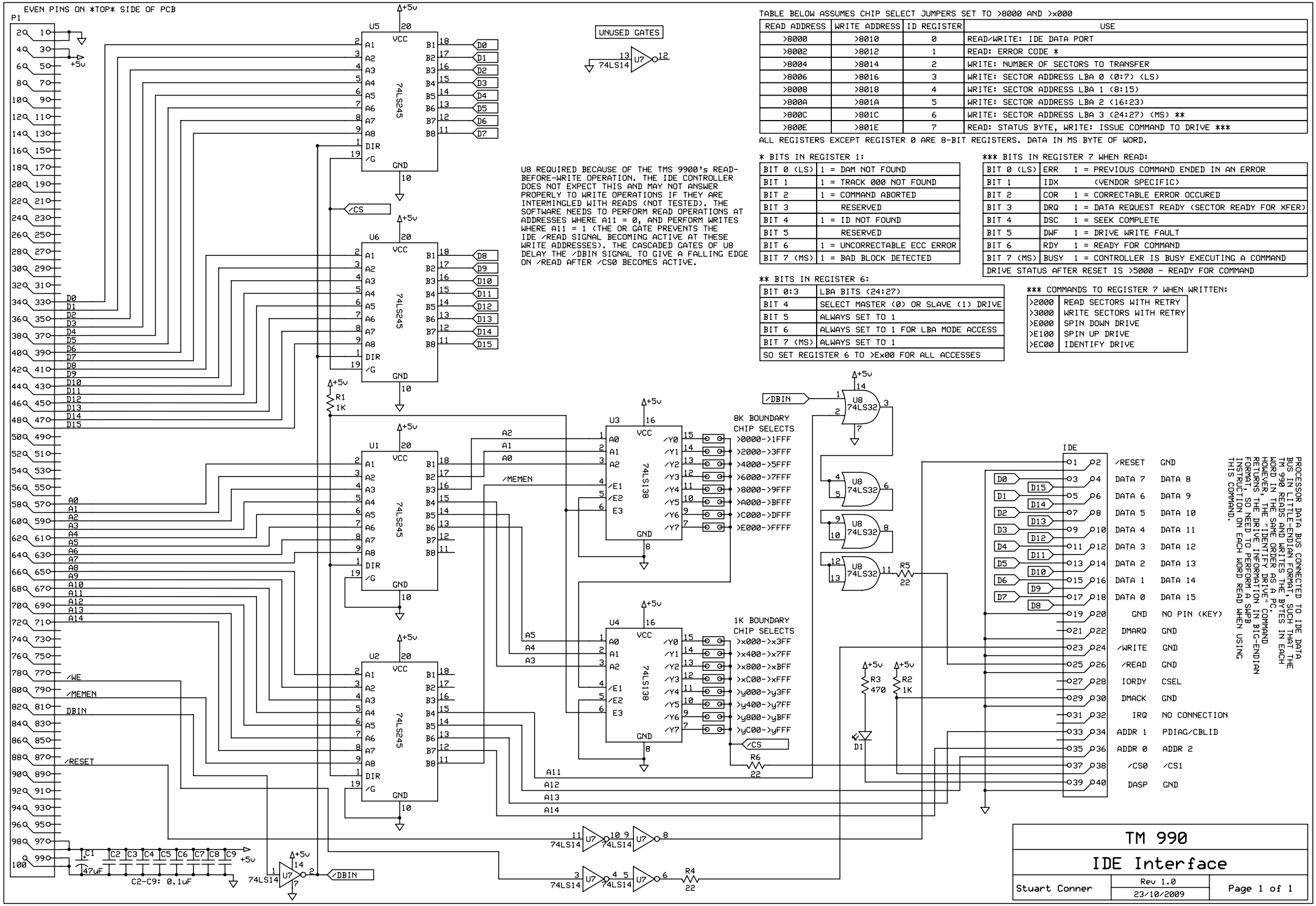

U8 REQUIRED BECAUSE OF THE TMS 9900's READ-BEFORE-WRITE OPERATION. THE IDE CONTROLLER DOES NOT EXPECT THIS AND MAY NOT ANSWER PROPERLY TO WRITE OPERATIONS IF THEY ARE INTERMINGLED WITH READS (NOT TESTED). THE SOFTWARE NEEDS TO PERFORM READ OPERATIONS AT ADDRESSES WHERE A11 = 0, AND PERFORM WRITES WHERE A11 = 1 (THE OR GATE PREVENTS THE IDE /READ SIGNAL BECOMING ACTIVE AT THESE WRITE ADDRESSES). THE CASCADED GATES OF U8 DELAY THE /DBIN SIGNAL TO GIVE A FALLING EDGE ON /READ AFTER /CS0 BECOMES ACTIVE.

TABLE BELOW ASSUMES CHIP SELECT JUMPERS SET TO >8000 AND >x000

READ ADDRESS	WRITE ADDRESS	ID REGISTER	USE
>8000	>8010	0	READ/WRITE: IDE DATA PORT
>8002	>8012	1	READ: ERROR CODE *
>8004	>8014	2	WRITE: NUMBER OF SECTORS TO TRANSFER
>8006	>8016	3	WRITE: SECTOR ADDRESS LBA 0 (0:7) (LS)
>8008	>8018	4	WRITE: SECTOR ADDRESS LBA 1 (8:15)
>800A	>801A	5	WRITE: SECTOR ADDRESS LBA 2 (16:23)
>800C	>801C	6	WRITE: SECTOR ADDRESS LBA 3 (24:27) (MS) **
>800E	>801E	7	READ: STATUS BYTE, WRITE: ISSUE COMMAND TO DRIVE ***

ALL REGISTERS EXCEPT REGISTER 0 ARE 8-BIT REGISTERS. DATA IN MS BYTE OF WORD.

* BITS IN REGISTER 1:

BIT 0 (LS)	1 = DAM NOT FOUND
BIT 1	1 = TRACK 000 NOT FOUND
BIT 2	1 = COMMAND ABORTED
BIT 3	RESERVED
BIT 4	1 = ID NOT FOUND
BIT 5	RESERVED
BIT 6	1 = UNCORRECTABLE ECC ERROR
BIT 7 (MS)	1 = BAD BLOCK DETECTED

** BITS IN REGISTER 6:

BIT 0:3	LBA BITS (24:27)
BIT 4	SELECT MASTER (0) OR SLAVE (1) DRIVE
BIT 5	ALWAYS SET TO 1
BIT 6	ALWAYS SET TO 1 FOR LBA MODE ACCESS
BIT 7 (MS)	ALWAYS SET TO 1
SO SET REGISTER 6 TO >Ex00 FOR ALL ACCESSES	

*** BITS IN REGISTER 7 WHEN READ:

BIT 0 (LS)	ERR	1 = PREVIOUS COMMAND ENDED IN AN ERROR
BIT 1	IDX	(VENDOR SPECIFIC)
BIT 2	COR	1 = CORRECTABLE ERROR OCCURED
BIT 3	DRQ	1 = DATA REQUEST READY (SECTOR READY FOR XFER)
BIT 4	DSC	1 = SEEK COMPLETE
BIT 5	DWF	1 = DRIVE WRITE FAULT
BIT 6	RDY	1 = READY FOR COMMAND
BIT 7 (MS)	BUSY	1 = CONTROLLER IS BUSY EXECUTING A COMMAND
DRIVE STATUS AFTER RESET IS >5000 - READY FOR COMMAND		

*** COMMANDS TO REGISTER 7 WHEN WRITTEN:

>2000	READ SECTORS WITH RETRY
>3000	WRITE SECTORS WITH RETRY
>E000	SPIN DOWN DRIVE
>E100	SPIN UP DRIVE
>EC00	IDENTIFY DRIVE

PROCESSOR DATA BUS CONNECTED TO IDE DATA BUS IN LITTLE-ENDIAN FORMAT, SUCH THAT THE TM 990 READS AND WRITES THE BYTES IN EACH WORD IN THE SAME ORDER AS A PC. HOWEVER, THE "IDENTIFY DRIVE" COMMAND RETURNS THE DRIVE INFORMATION IN BIG-ENDIAN FORMAT, SO NEED TO PERFORM A SWPB INSTRUCTION ON EACH WORD READ WHEN USING THIS COMMAND.

TM 990

IDE Interface

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